Comprehensive Optimization Method for Thermal Properties and Parasitics in Power Modules

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Abstract—A combined optimization approach regarding thermal properties and parasitic elements inside power semiconductor modules for power electronic converters is presented. The proposed method allows the determination of the best suited semiconductor positions on the DBC substrate as well as optimization of the substrate structure. The optimization procedure leads to a matrix representation illustrating the results in a concrete way.

Keywords—Thermal design, EMC/EMI, Packaging, Simulation

I. INTRODUCTION

Due to the ongoing increase of power density in power modules for power DC to AC converters the coupling between thermal properties and parasitic elements becomes more and more relevant. Optimization of the DBC (direct bonded copper) layout and the chips’ positions in these modules helps to improve the electro-thermal performance and to enhance reliability. Several investigations have been made to find optimal layouts for the reduction of stray inductance [1], [2] or to increase the cooling efficiency [3]. For comprehensive optimization the coupling of electrical and thermal properties inside power modules has to be considered, i.e., a large distance between chips improves the heat spreading, but the stray inductance of the module increases due to the necessarily longer commutation path. The use of broad tracks reduces stray inductances [4], however parasitic capacitances increase at the same time [5]. These examples show that the optimization process of power modules is a nontrivial task, as the demands for optimization are contradicting.

Suggestions for a combined optimization approach have been made [6], [7]. In [6] the optimization process involves thermal behavior and parasitic capacitors, whereas inductance is neglected. A complex numerical algorithm restricted by an extensive set of boundary conditions was used. [7] mainly focuses on thermal issues and parasitic inductances. The thermal issues are investigated first, parasitic inductances are optimized in a second step.

This paper proposes another systematic approach for a combined optimization process for power modules. It has the benefit of being very concrete and applicable without the necessity for a major programming effort. Different optimization targets can be investigated within one overall model. The approach can be generalized to arbitrary layouts and different boundary conditions. The method is presented based on simulation. All simulations were carried out by means of the software INCA3d [8] and Comsol Multiphysics [9], using PEEC and FEM algorithms, respectively. A simple MOSFET half-bridge configuration is used as an example, but the stated methods can be used for other circuits as well. Following this introduction a systematic approach for power module design is stated. The third part introduces an exemplary half-bridge optimization problem that is solved with the suggested approach in the fourth section. In the fifth part the overall performance is evaluated and the paper is finished with the conclusion.

II. SYSTEMATIC OPTIMIZATION APPROACH

The systematic optimization approach consists of three steps: first, the basic boundaries for the layout of the DBC are determined. Therefore the minimum required surface area and cross-section of the copper areas on the DBC are assigned. They arise from thermal spreading requirements and the intended minimization of copper losses.

Additionally, assembly constraints such as that on the minimal distance between components and edges of the DBC and the placement and size of the pads for power terminals and gate contacts define the DBC size. In the second step, all eligible power semiconductor positions are evaluated and the electro-thermal optimization is carried out by means of simulation. In the third step, the final DBC structuring is done, following common design rules for the minimization of parasitic elements [4], [5]. For the evaluation of the ideal semiconductor position, all suitable positions for chip placement on the copper tracks are evaluated. Within the resulting areas, a fine grid of equidistant points is defined, representing the possible center points of the semiconductors. For each point, the thermal properties, the parasitic inductances consisting of DBC inductance and bond wire inductance, and the parasitic capacitances are simulated. The results for each parameter are stored within a matrix. Thus, every parameter to be optimized has its own matrix. The matrix elements represent the discrete values for the according chip position and can be visualized in a two dimensional plot. The matrix elements are standardized and a weighted
summation of all matrices (with weight factors $w_i$) can be carried out, leading to the optimization matrix providing instantaneously a result for an optimal semiconductor placement, combining thermal and parasitics optimization. Fig. 1 presents the schematic flow diagram for this optimization.

In the last step, the final DBC structuring is carried out, aligning with the final semiconductor positions. This structuring defines the area of the copper tracks, influencing the parasitic capacitances as the potentials of the phase track changes with time.

The analysis of the optimization process through a two dimensional graphical matrix representation has additional benefits, i.e. it allows the definition of an acceptance range for each parameter, leading to the definition of tolerance zones for the chip position, depending on the parameter. Additionally, the matrix can be used to obtain an estimation of the success of the optimization, as the theoretical possible minimum and maximum values for each parameter are evidently given. The proposed approach is demonstrated on an exemplary power module in the next chapter.

III. OPTIMIZATION OF A HALF-Bridge POWER MODULE

The fictive half-bridge power module (Fig. 2) investigated here is chosen to show the optimization process for a simple geometry. The points to start from are the given technical and geometrical boundary conditions.

The minimum size of the module is given through thermal boundaries, as there are given demands on heat spreading and minimization of copper losses, defining the surface area needed and the cross-section of the copper tracks required. Here, the boundary conditions given by assembly constraints like the minimal distance between components and edges of the DBC and the minimal size of the pads for power terminals and gate contacts could only be given marginal consideration. First, the minimal required DBC size is estimated based on the given thermal boundary conditions and thermal constraints. For the given example a minimum of 720 mm$^2$ is specified. This arises from the sum of the areas of the chips (60 mm$^2$ each), the targeted filling degree of 25%, the estimated space required for the terminal contacts and to comply with the necessary distance between components and edges of the copper tracks respectively. The degrees of freedom for reshaping and optimization of this layout have to be well-known. Being restricted for this example by the given assembly limitations and the convention that DC and phase tracks have to be on opposite sides of the module, the prospects for variation of geometrical shape and component placement are shown in Fig. 2 as green arrows. The position of the high-side power semiconductor, here a MOSFET is taken for example, in the lower left corner was previously defined by analytical considerations, as the position close to the positive DC-track accounts for a short commutation path and therefore low stray inductance. The distance of 2 mm to the edges of the DBC guarantees good heat spreading [10]. The placement of the second semiconductor (low-side MOSFET) is more difficult as it is influenced by the thermal coupling with the other MOSFET. The optimization of its position on the track is shown in the following.

<table>
<thead>
<tr>
<th>Table I</th>
<th>THERMAL PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>60 mm$^2$</td>
</tr>
<tr>
<td>DBC Size</td>
<td>720 mm$^2$</td>
</tr>
<tr>
<td>DBC Stack (Cu/Al$_2$O$_3$/Cu)</td>
<td>300$\mu$m / 400$\mu$m / 300$\mu$m</td>
</tr>
<tr>
<td>Base Plate (area/thickness)</td>
<td>1280 mm$^2$ / 2 mm</td>
</tr>
<tr>
<td>losses of each chip</td>
<td>30 W</td>
</tr>
<tr>
<td>ambient temperature</td>
<td>300 K</td>
</tr>
<tr>
<td>htc (heat sink)</td>
<td>$h = 500$ W/m$^2$K</td>
</tr>
</tbody>
</table>

A. Thermal Optimization

The requirement for a thermally optimized module is to exhibit a low thermal resistance $R_{th}$ to the ambient, acceptable maximum temperature $T_{max}$ during operation and a low temperature gradient $\Delta T$ on the DBC.
The relevant constraints are the shape of the copper tracks, the thickness of the substrate, and the location of the semiconductors. With [11] the minimal thermally required copper area for a single chip can be calculated. If more than one chip is placed, the thermal coupling has to be considered, too. In the selected example, the two MOSFETs both exhibit a chip area of 60 mm$^2$. For the simulations performed with Comsol Multiphysics [9], total losses are assumed to be of 30 W each. The thermal stack is shown in Fig. 3. The DBC (30 mm x 24 mm) consists of the upper copper layer with thickness of 300 µm, the Al$_2$O$_3$ ceramic of 400 µm and the backside copper metallization of 300 µm. The DBC is mounted on a copper base plate (40 mm x 32 mm) with a thickness of 2 mm and cooled by an arbitrary heat sink of the same base area, simulated through an extended surface heat transfer coefficient ($htc$) $h = 500$ W/m$^2$K. Only the steady-state condition is regarded here.

From the thermal optimization point of view, a low and isothermal temperature all over the DBC is beneficial, as it avoids hotspots and allows good heat spreading and cooling. Therefore the deviation from an isothermal DBC is investigated. This means the difference in DBC surface temperature is calculated $\Delta T = T_{DBC,max} - T_{DBC,min}$ for possible semiconductor positions, where $T_{DBC,max}$ is the junction temperature found in the center of the MOSFETs. Simulations of possible semiconductor positions and their graphical appearance are shown in Fig. 4. Blue indicates low temperature, red, high temperature. The matrix values are only shown for areas suitable for semiconductor placement, i.e. the phase track. It can be seen that from a thermal point of view, the best place for semiconductors would be close to the center of the copper area, shifted a little to the upper right for reducing thermal coupling to the first chip located close to the lower left corner.

**B. Stray Inductance Optimization**

The second property to optimize is the stray inductance of the power module. They should be kept below an acceptable value. In case of the half-bridge configuration the general aim for this is to keep the commutation path short. The length is affected by the position of the second MOSFET, hence its particular influence on the modules inductance is investigated in this section. For an estimation of the overall stray inductance the terminals inductances and the fraction of the high-side bond wire connection have to be added. The current is guided to the semiconductor in two layers: The substrate metallization on the one hand, and the top side connection by bond wires on the other. This has to be taken into account when calculating the inductance values for each possible chip position of the low side MOSFET. Fig. 5 shows the DBC stray inductance simulations for variation in chip positions on the copper metallization. Blue indicates low and red indicates high stray inductance. It is obvious that semiconductor placement on the lower left corner would minimize stray inductance contributed by the phase track, as the current path through the two semiconductors is short when placed close together.

Fig. 6 shows the stray inductance for the bond wire connections. It can be seen, that the fraction of the bond wire stray inductance increases with the distance to the negative DC track in a radial manner. The bondwires exhibit a larger stray inductance compared to the current path through the substrate in general, because they have smaller cross-section and are spanned as an arc, thus having increased length.

By plotting these values, the given visualization is made, simplifying the optimization of stray inductance by indicating suitable chip positions.

**C. Capacitance Optimization**

The third characteristic to optimize is the stray capacitance. This is responsible for the amount of common mode interference [6] and should be reduced to low, acceptable values. The capacitance is influenced by the thickness of the substrate and the size of the copper area of the tracks. The capacitance of the phase track is the most relevant, as its potential is fast changing within every switching operation, while the DC tracks have the fixed potential of the DC link. Thus the primary aim is to reduce the copper area of the phase tracks and to
enlarge the thickness of the substrate, but this contradicts the requirements of thermal optimization as the Al₂O₃ ceramics exhibit poor thermal conductivity (20-170 W/mK) compared with the copper layer (395 W/mK) [12].

Fig. 7 (a) shows the decrease of calculated parasitic capacitance for substrate thickness increasing from 200 μm to 1200 μm for a copper area size of 500 mm². Fig. 7 (b) shows the linear correlation between capacitance and decreasing size of the copper area starting from the maximum (500 mm²) to the lowest possible value (150 mm²) in the given example.

As not all substrate thicknesses are commercially available we concentrate on the thickness of 400 μm which is widespread and offers good thermal performance. Thus the size of the phase track copper area is the major variable of interest. As seen in Fig. 7 (b), the optimization can be done by downsizing the phase track: the smallest size yields the lowest capacitance.

Placement of the low-side MOSFET close to the phase terminal (right side of Fig. 8) allows the reduction of the size of the phase track copper area. The optimization can be found by calculating the required copper area for a set of possible chip positions, thereby the phase track length is shortened linearly, while the width is kept constant.

IV. COMBINED OPTIMIZATION

The results from the last section have to be combined, taking all couplings into consideration. In the previous section the optimal semiconductor placement depending on the corresponding parameter was calculated. All simulated values are given in one matrix for each parameter: \( M_{\Delta T}, L_{\text{sub}}, L_{\text{bond}}, \text{Capacitance} \).

The idea of the combined optimization approach discussed here is to perform a weighted summation of these matrices, where the weighting factors are defined by the demands of the application. Before this summation can be carried out, the matrices have to be standardized in order to be comparable. Therefore, the elements of each matrix are scaled to values between 0 and 1, where 0 represents the minimum and 1 the maximum value of the particular matrix. The matrix summation leads to the optimization matrix \( A \) depending on the weighting factors \( w_i \), where \( \sum w_i = 1 \) is defined as follows:

\[
A = w_1 \cdot M_{\Delta T} + w_2 \cdot L_{\text{sub}} + w_3 \cdot L_{\text{bond}} + w_4 \cdot C
\]

The weighting factors can be given as percentage values. Figure 9 demonstrates the results of a combined optimization of thermal, inductive and capacitive properties. All these parameters are equally weighted in this example. Blue indicates optimal chip position under these boundaries. If the power module application requires an emphasis on one special feature, the weighting can be changed to prioritize specific optimization matrices, or to exclude applications depending on negligible parameters.

Fig. 10 shows the optimization results for the assumption of an exemplary power module using low voltage MOSFET, where stray inductances are a major concern in module design. Therefore the optimization weighting is chosen as follows: 80% stray inductance, 10% thermal performance, 10% stray capacitance.

A high voltage application might focus more on thermal issues and stray capacitance, which can easily be investigated by changing the weighting to: 10% stray inductance, 60% thermal, 30% stray capacitance. This result is shown in Fig. 11. Another approach for chip placement is to define regions of acceptance for each parameter and to find the intersection of these areas for placing the semiconductors in acceptable areas.
V. Evaluation of Overall Performance

The last step of the optimization process is to estimate the total performance of the power module using the optimized parameters. This can be done by using the results found in Chapter III from which the theoretical optimum for each single parameter is known. To get an idea of the expected values for thermal and electric properties, they are derived from the-appropriate matrices for the chip positions found in Chapter IV. Table II shows the resulting values for the optimization boundaries given in Fig. 9, Fig. 10 and Fig. 11. They show, for the equal weighted optimization of the power module, values close to the mean value of the particular value.

The stray inductance optimization (case 2) leads to noticeably lower values for $L_{\text{sub}}$ and $L_{\text{bond}}$, but higher values for $C$ and $\Delta T$. While in the high voltage model (case 3) a low $\Delta T$ is achieved and low $C$. This is beneficial for high voltage MOSFET as high $dU/dt$ occurs during switching processes and hence common mode noise occurs if stray capacitance is too high. These examples show the practicability of this method for a combined optimization approach. Other examples can be calculated depending on the demands of the intended application.

<table>
<thead>
<tr>
<th>Optimization Demand</th>
<th>Estimated Values</th>
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<tbody>
<tr>
<td>$w_{M_{\Delta T}}$</td>
<td>$w_{L_{\text{sub}}}$</td>
</tr>
<tr>
<td>25%</td>
<td>25%</td>
</tr>
<tr>
<td>10%</td>
<td>40%</td>
</tr>
<tr>
<td>60%</td>
<td>3%</td>
</tr>
</tbody>
</table>

VI. Conclusion

A combined optimization approach regarding thermal properties, stray inductances, and stray capacitances inside power semiconductor modules was presented. The method allows the finding and comparison of the best suited positions for power semiconductors on the DBC substrate as well as an optimization of the substrate structuring. The results of the optimization are given in a matrix representation illustrating the performance achieved in a concrete way.

Different optimization tasks can be carried out in one complete model consisting of the single optimization matrices with the feasibility for a parameter dependent weighted optimization or the optimization with the assignment of tolerance areas for chips positions. This approach has the advantage of being simple to use and might be an aid to guide development engineers on the way to an optimized power module.

For obtaining the optimization matrices it is advantageous to use a software algorithm varying the chip positions automatically, calculating all parameters in one cycle.

For a generalization of the proposed method for multichip power module optimization it is required to find an adapted approach. A practicable way might be to add chips successively to the DBC, repeating the steps described in this paper after every semiconductor placement. The investigation of this is still in progress.

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REFERENCES


