Optimization of the Stray Inductance in Three-Phase MOSFET Power Modules Aided by means of PEEC Simulation

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Keywords

<<EMC/EMI>>, <<Automotive application>>, <<MOSFET>>, <<Design>>

Abstract

Minimum stray inductances are of high importance for power modules and stacks of converters. This paper describes the optimization of the stray inductance for a compact DBC based three-phase power module for use in 5 to 20 kW converters for automotive application. The inductances of different DBC layouts and mounting technologies are compared and optimized, including chip connection with soldered tapes. The simulated values are compared with measurement results.

Introduction

Power converters for automotive application with electrical drives in the engine power class from 5 to 20 kW will be needed more and more in future. Common application today is found in lift trucks or other automotive domains. Powered by lead-acid storage batteries with 24 V DC link voltage, these converters have to produce three-phase currents of 100 to 500 A (RMS). Converters including power modules with applicable topologies are widespread. These modules are in the majority build with MOSFET on DBC substrate (Direct Bonded Copper) where the top sides of the chips are connected using bond wires. To reduce losses they are operated using short switching time, likely below 200 ns.

On the other hand overvoltage and EMC problems increase with decreasing switching time, especially the stray inductance of the DBC becomes an important value to be considered. Minimization of the stray inductance leads to less induced overvoltage allowing the use of MOSFET with lower breakdown voltage and hence lower $R_{DS(on)}$. Thus, low stray inductance of power modules reduces both: switching losses due to the possible lower switching time as well as losses caused by semiconductor resistance due to devices with lower breakdown voltage. All together that leads to higher efficiency and smaller amount of heat produced by the MOSFET ending up in smaller and cheaper converters, as heat sinks and cooling efforts can be minimized. It is obvious that an inductance-optimized module will additionally reduce interference in the DC link and save costs for additional EMI protection and filter electronics.
Until now only few publications dealing with stray inductance in three-phase MOSFET power modules can be found [1, 2]. Most publications concentrate on the analysis of subdomains in the module, like the optimization of gate circuit layout [3]. Comprehensive analysis can be done by modeling and simulation of the whole module with its conductors in their mechanical setup, which is presented here. The use of the partial element equivalent circuit method (PEEC) allows the modeling and simulation of complex module topologies accounting bond wires for the top side connection of chips and diodes. By this, values for the stray inductance, the current distribution, losses and Lorentz forces can be deducted.

Despite the calculation using PEEC simulation technique it is essential to choose the right methods for verifying the results. Measurement of inductances in the range of 1 to 50 nH, which is the common value for power modules, is a challenging task. A frequency shifting oscillator was built and used for the measurements.

In this publication a module containing a three-phase MOSFET bridge for 24 V battery voltage application and currents up to 150 A is investigated concerning stray inductance and its optimisation. First, a short overview on DBC topology and design requirements is given, followed by an estimation of allowable inductance for the assumed case. Then, four different layout approaches will be presented and compared in means of simulation and evaluating measurements allowing to find the optimal module. At the end, a conclusion is given.

### DBC Topology and Design

#### Topology and Requirements to Stray Inductance

Designing a power module DBC layout means to transfer the ideal schematic to a real circuit. Here it is additionally required to follow design rules leading to small stray inductance. Figure 1 gives a simplified overview illustrating parasitic inductances.

The commutation path describes the current flow inside the module when one MOSFET is switched off and the freewheeling diode of the same half bridge takes the current. In the given example (Fig. 1) assume V1 to be initially switched on. When V1 switches off, the freewheeling diode of V4 takes the current. Due to the decay of the current through V1 the parasitic inductances $L_{DC^+}$, $L_{V1S}$ and $L_{V1D}$ create an induced overvoltage. The increasing current in the freewheeling diode on the opposite side creates induced voltage due to $L_{DC^-}$, $L_{V4S}$ and $L_{V4D}$. The inductance of the phase conductors is not part of the commutation path, because the current stays nearly constant due to the high inductance of the motor (not shown). Thus it is necessary to reduce stray inductance of the module layout as well as providing a low inductive connectivity to the DC link.

![Figure 1: Parasitic inductances of a three-phase power module](image)

#### Design of Module Layouts

Three-phase power modules have two DC tracks where the DC link voltage is applied and three phase tracks that carry the current out of the module to the motor. The 6 MOSFETs chips are placed on the tracks with positive potential, the drain contact is on the bottom. Source and gate contacts are connected by bonds or by soldered tapes in this case. The aim is to carry the DC link voltage to the phase tracks...
in a way that allows high symmetry, ease of assembly and low parasitic inductance, while providing sufficient space for the chips. Among several different approaches the following will present four exemplary options to realize a three-phase MOSFET power module DBC layout in the size of $2000 \text{ mm}^2$ (i.e. $50 \times 40 \text{ mm}^2$).

The designs examined have in common that using a symmetric layout is of central interest. This leads to symmetric current distribution as well as to symmetric stray inductance in the three-phase system. Furthermore the ease of assembly is an aspect even more important as low stray inductance and is therefore kept in mind during the design process. The aim is to achieve a chip size of $60$ to $80 \text{ mm}^2$ which has shown to be best trade-off between the ability of carrying high currents, low losses and thermal aspects like homogeneous heat distribution and thermo mechanical stress in the module [4].

The first layout (tab. I) shows a symmetric DBC layout with the DC link connected to the outer tracks. The three phase contacts are placed in between a loop spanned by these DC link tracks. The three phase contacts are guided to the upper side of the module by tapes above the negative potential of the DC link. There are $15$ tapes needed to realize topside connection to the chips.

The second layout provides a smaller loop of the DC track by breaking the concept of placing power and controlling contacts on different sides of the module. Keeping the DC track short is the first optimization step. Additionally a total number of six tapes is sufficient which also decreases stray inductance. Here the three phase contacts are at the upper side, while DC link and controlling contacts are placed at the lower side.

The third layout reduces the loop of the DC track compared to the previous designs. The DC link tracks are in the center of the module. Antiparallel currents lead to inductive counter coupling reducing stray inductance. The high side chips are placed on the positive DC track, the low side chips on the phase tracks, keeping the current path nearly equal for all three phases.

The fourth layout shows a complete different approach; here a 3D-geometry is analyzed, allowing to reduce the length of the current path drastically. A multi-layered approach for IGBT module has also been presented by [5]. Here, the chips are placed on the bottom DBC and the three phase conductors are built on their top by applying copper bars. The high side chips are placed on these phase bars and the top
DBC is the same as the bottom. This layout combines the benefits of broad tracks, antiparallel currents for inductive counter coupling and a short DC track avoiding bond wires. High symmetry is achieved with this layout, but the challenge lies in the structural-design technology.

**Estimation of the allowable inductance**

The MOSFET chips used as base for design have a breakdown voltage of 60 V, reducing $R_{DS(on)}$ to values of less than 2 mΩ, like the International Rectifier IRIRLS3036. DC link voltage is 24 V, which can increase to maximum voltage of 36 V during battery charging due to power management. The required safety clearance for the MOSFET is set to 25% that is 15 V. Summing all together there is only 9 V left for allowed voltage induction due to stray inductances. Maximum allowed inductance for the commutation circuit can easily be calculated.

Since the peak currents of 150 A for one module are a fixed value, only the switching time can be varied in order to stay below the allowed overvoltage for a given inductance. Assume a designated switching time of 150 ns, then inductance must be below 10 nH. Converters with higher power class will use two or more paralleled modules. By paralleling modules overall current increases linear, but effective inductance decreases the same factor, therefore the induced voltage stays nearly constant. In the given example the aim is to design a module with less than 10 nH stray inductance. Parasitic capacitors are of minor importance at the given conditions. As an example imagine the whole module as a plate capacitor with 2000 mm$^2$ at a distance of 0.4 mm and $\varepsilon_r \approx 10$. The capacitance is calculated to 0.4 nF, this results in a displacement current of about 100 mA. Compared to a current of 150 A this effect is negligible small.

**Simulation**

**Stray Inductance**

Partial element equivalent circuit method, carried out by Cedrats InCa3D software, is used to model and simulate the different layouts [6, 7]. Complex geometrical structures are simulated numerically by automatically subdividing the cross-section in rectangular basic elements. For these elements a current distribution is deducted in the software allowing the determination of the magnetic field and thereby of the stray inductance.

The simulation calculates the stray inductance measured between the terminals of the positive and negative DC tracks. Each module offers different possible commutation paths, therefore the one with the highest stray inductance is chosen for simulation, which is the central commutation path (phase v) for the modules examined.

Figure 2 shows the result of the stray inductance simulation of module 1 for the path defined by one half bridge in tab. 1. Frequencies of 2 to 8 MHz are examined. This is the sine wave approximation to the related switching time (43 - 175 ns). It can be seen that inductance is almost constant in that frequency range, due to the fact that current distribution affected by skin and proximity effect stays nearly constant. Hence frequency dependence can and will be neglected.

![Figure 2: Frequency dependence of stray inductance for module 1](image)

The simulation reveals an inductance of 24.6 nH for the first layout. This high value results from the large loop spanned by the DC link guided around the three phase tracks in the center of the DBC. This loops encloses the whole area of the module.
The shortening of the DC link track in the 2nd layout and the reduction of tapes (6 instead of 15) decreases the inductance to 17.3 nH. In the 3rd layout the DC link is placed in the center of the DBC, surrounded by the three phase tracks. Tapes are short and high symmetry of different commutation path is achieved. That results in inductance as low as 10.2 nH and in a more balanced current distribution. Using the three dimensional stack in layout 4 reduces inductance to values of 5.4 nH, simultaneously doubling the usable surface for chip placement. Figure 3 shows the inductance values from simulation. From the inductance optimization point of view this layout presents the optimum, but stacks as in the 4th layout put high demands on packaging in industrial assembly. Therefore the 3rd layout is the best trade-off of the presented designs between achieving low stray inductance and low assembly costs.

![Figure 3: Stray inductance of our power module layouts (simulation)](image)

**Switching Performance**

Figure 4 shows the PSpice simulation of a switching-off process simulated with an equivalent circuit accounting the stray inductance of the commutation path. The voltage-current waveform is for a 25 nH power module (layout 1) compared to a 10 nH module (layout 3) with a MOSFET chip switching off 150 A in 150 ns. The maximum voltage is roughly 49 V for the 25 nH module and 37 V for the 10 nH Module. The aberration compared to analytic calculations via the formula $U_{\text{ind}} = L \cdot \frac{dI}{dt}$ is due to non-linear current waveform in the switching process. Oscillations are due to the LC circuit given by gate-drain and drain-source capacitances and the stray inductances.

![Figure 4: Switching-off performance of the power MOSFET-Module (150 A current (red), switched off in 150 ns, for a commutation stray inductance of 25 nH (blue) respectively 10 nH (green))]([image]

**Inductance measurement**

All simulated data have to be verified using an adequate measurement method. In this case inductances of 1 to 100 nH has to be measured. The required accuracy is set to 1 nH. Keeping in mind that a single wire of 1 cm length has an inductance of about 10 nH exact measurement is challenging. Due to the absence of an accurate LC meter a self-build device is used, according to the proposal of [8] and [9]. A frequency shifting oscillator is used for the measurements. It consists of a 650 kHz oscillator built with a LC circuit [10].
After startup the natural frequency of the LC circuit is measured with a micro controller. This frequency is stored \((f_1)\). In a second step a calibration capacitor of well-known capacitance is paralleled to the circuit. The resulting frequency is measured and stored \((f_2)\). Now the calibration capacitor is disconnected again and the unknown inductance (the module) is paralleled to the circuit, obtaining frequency \(f_3\). Now there are three different frequencies and the known capacitance. Thereby the unknown inductance \(L_x\) can be calculated via \([10]\):

\[
L_x = \left[ \left( \frac{f_3}{f_1} \right)^2 - 1 \right] \cdot \left[ \left( \frac{f_3}{f_2} \right)^2 - 1 \right] \cdot \frac{1}{C_{cal}} \cdot \frac{1}{(2\pi f_1)^2}
\]

The advantage of this setup is that the influence of the measurement wires’ stray inductance can be excluded by shorting these wires during calibration prior to module inductance measurement. By doing this the wire inductance is added to the LC circuit of the measurement device. The natural resonance frequency calculated on startup thereby includes the parasitic inductance of the wires. This setup is capable of measuring inductances of 1 to 100 nH with good resolution (+/- 1 nH).

Due to the fact that industrial fabrication of power module DBC is expensive and can only be done in mass customization, cheaper and easier to build alternatives are required for the exploratory analysis. Therefore modules based on printed circuit boards (PCB) have been built up and were used for measuring the stray inductance.

The module test samples are not assembled with chips, only copper tapes are soldered on the surface of the modules, forming an exemplary commutation path. Thus the modules do not have electrical functionality so far, but they could be used for valuating measurements of parasitic inductance. Out of the different possibilities for commutation path the worst case is analyzed. That is the one with the longest DC link track.

Since the measurement only needs current in the mA regime, it is not necessary to use thick copper tracks. The module test samples are a good approximation to the DBC modules regarding measurement of parasitic inductance. Three of the four modules have been build up as test modules in the way described: Table II shows the measurement results. They correspond well to the simulated ones.

### Comparison of the Module Designs

Modules 1 and 2 exhibit high stray inductances, due to long DC tracks and high number of tapes in case of module 1. Module 4 shows lowest inductance. As it requires a three dimensional stack of MOSFET chips and copper tracks it cannot be assembled with nowadays packaging methods. The concept might be interesting for future projects. Module 3 gives the best tradeoff between low inductance on the one hand and ease of assembly on the other hand. This layout has combined the requirements of short DC tracks, small number of bond wires and uses broad tapes at the same time allowing low inductive connection to the DC bus bar.

<table>
<thead>
<tr>
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<th>Module 1</th>
<th>Module 2</th>
<th>Module 3</th>
<th>Module 4</th>
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<td>length of DC track</td>
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<td>width of tracks</td>
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<td>+</td>
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<tr>
<td>number of tapes</td>
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<td>bus bar connection</td>
<td>+</td>
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<td>ease of assembly</td>
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<td>17.3 nH</td>
<td>10.2 nH</td>
<td>5.4 nH</td>
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<td>15 nH</td>
<td>11 nH</td>
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Table II: Overview of the modules’ characteristics. Valuation is good, fair or poor: + / o / -.

(*Module 4: not producible)

### Conclusions

The analysis and optimization of the stray inductances in a three-phase MOSFET power module has been presented. The module taken for analysis is small in size (2000 mm²) and allows the use of large chips (55 to 100 mm²). It is based on a DBC substrate but can also be built with lead frame technology. The module is designed for automotive applications with 24 V DC link voltage and 150 A current.
Four different layouts have been compared to each other, revealing assets and drawbacks of different approaches. Simulations with partial element equivalent circuit method have been carried out to model and simulate the DBC layouts. An iterative optimization process has been chosen to achieve lowest possible inductance. Starting from 25 nH the stray inductance could be reduced to 10 nH.

Simulation has helped to discover methodologies to reduce the stray inductance of power modules. Some useful design rules were derived: Keeping DC tracks short, minimizing number of bonds and the use of broad tapes and copper tracks on the DBC. During development of a power module a trade-off between optimizing stray inductance and fabrication possibilities is required. For this reason a three dimensional layout is not competitive, although it has the benefit of lowest inductance.

The simulation results for the exemplary modules have been verified using a self-build LC meter capable for measurement of small inductances in the nH-range. The measurements sustain the simulated data. The fabrication of electrical functional demonstrator modules is outstanding and will be the next step.

References