Comparison of a Z-Source Inverter and a Voltage-Source Inverter Linked with a DC/DC-Boost-Converter for Wind Turbines Concerning Their Efficiency and Installed Semiconductor Power

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Abstract—In this paper the power losses of both Z-source-inverter (ZSI) and voltage-source inverter linked with a dc/dc boost inverter (VSI+BC) are compared. Therefore the circuits are simulated in time domain by means of numerical methods whereas the switching and conducting losses are calculated separately and in parallel. A main focus is on mathematical description of the current rms through the IGBTs of the ZSI to derive the conducting losses. It is shown that the losses of the diode in the dc link of the ZSI has a high percentage of the total power losses and cannot be neglected. Besides that the choice of the modulation method has a high influence on the power losses of the ZSI as well. Based on the calculated power losses the efficiency and the installed semiconductor power are investigated and compared for different input voltages. The results show that for an output voltage of 400 V the VSI+BC topology outperforms the ZSI in almost all operating points. The reason is that for low input voltages the VSI+BC topology boosts the input voltage to limited 600 V and the VSI works with a modulation index of about 1 very efficiently. However the ZSI has to boost the input voltage to much higher values, since for high voltage gains long shoot-through-states are essential. However, long shoot-through-states are coming along with long zero-states which causes a buck behavior.

I. INTRODUCTION

The Z-Source-Inverter (ZSI) is a promising new inverter that has been discussed in several papers [1][2][3]. It is suitable for similar applications as a three phase voltage source inverter linked with dc to dc boost converter (VSI+BC) [4][5]. Both topologies are able to boost a low dc voltage and invert it to a three phase voltage. Possible applications for both inverters are connecting fuel cells, photovoltaic cell or wind turbines with synchronous machines to the grid. In [4], [5] and [6] comparisons between these two topologies have been presented. In addition, this paper deals with the power losses of all semiconductor devices, including the diode in the dc link. A new approach of calculating the effective power losses of VSI+BC and the ZSI are presented, respectively. Based on these results the efficiency and the necessary installed semiconductor power of both topologies is derived for a wide range of different input voltages and finally compared to each other. For the derivation of the equations which are describing the losses of the ZSI very extensive calculation have been done which cannot be presented in this paper due to the limited space. The derivations will be presented in another publication.

The paper is organized as follows: In section II the system configuration and control is described. The third section deals with general modeling of power losses in semiconductors. In sections IV and V the power losses of the VSI+BC and the ZSI are evaluated respectively. In the next section efficiency and installed power semiconductor rating are introduced. In section VII the method of simulation is described while in VIII the possibility of comparing both topologies is discussed. After that the ZSI is compared to the VSI+BC concerning power losses efficiency and installed semiconductor power. Finally the results are summarized in section X.

II. SYSTEM CONFIGURATIONS AND CONTROL

In this paper the benefits of the VSI+BC and the ZSI are compared. The investigated application is to feed in energy from a dc source (V_in), represented by a wind power generator with rectifier for example, to the three phase ac grid. Their topologies are shown in figures 1 and 2. The voltage source inverter is controlled by means of vector modulation. The boost converter in the dc link provides a voltage V_C that is high enough to let the VSI provide the required output voltage with a modulation index near 1 to achieve its best efficiency [7]. The ZSI is controlled by a modified vector modulation and outputs a required voltage by adjusting the length of the shoot-through duty cycles [5][8]. The shoot-through states are placed instead of the zero states while the active states are the same as for traditional voltage source inverter. The length of the shoot through states increases with the ratio between the input and the output voltage so that a voltage gain can be achieved. If a buck behavior is desired
The conduction losses are small and can be neglected [9]. In the following the switching losses are considered as well as the driving losses. Compared with the conduction and off-state losses as well as switching and driving losses are very small and can be neglected [9]. In the following the forward or conducting characteristics of the semiconductors have been linearized. The conduction losses $P_C$ are calculated by (1) and (2) for one IGBT and one diode and depend on the mean and the rms values of the current $i_c$ through the valves. $V_{CE,0}$ and $V_{F,0}$ describe the threshold voltages and $r_{CE}$ and $r_F$ the differential ohmic resistances of the IGBT and the diode, respectively.

\[
P_C^{\text{eff}} = V_{CE,0} I_{c} + r_{CE} I_{c}^2 \quad (1)
\]

\[
P_C^{\text{disc}} = V_{F,0} i_{c}^2 + r_{F} i_{c}^2 \quad (2)
\]

The switching losses are a function of the switching frequency, voltage and current. However they depend also on the chosen PWM-method and the switching loss energies of the IGBT ($E_{on}$, $E_{off}$) and the diode ($E_{on}$). In datasheets these information are only given for a reference voltage $V_{ref}$ and a current $I_{ref}$. In (3) and (4) the switching power losses are given for the continuous PWM depending on actual voltage $v_c$ and current $i_c$.

\[
P_{\text{SW,cont}}^{\text{IGBT}} = \frac{1}{\pi} \int \left( E_{on} + E_{off} \right) \frac{v_c}{V_{ref}} i_c \quad (3)
\]

\[
P_{\text{SW,cont}}^{\text{Diode}} = \frac{1}{\pi} \int E_{on} \frac{v_c}{V_{ref}} i_c \quad (4)
\]

To reduce the switching losses a discontinuous PWM might be used. In this case the valve that is carrying the greatest current is permanently turned on for a sixth of a line period. In accordance to [11] and as long as $|\cos \varphi| < \frac{\pi}{6}$, the switching losses are halved to the standard PWM because the number of switching events and switching power is reduced:

\[
P_{\text{SW,cont}}^{\text{IGBT}} = \frac{1}{2\pi} \int \left( E_{on} + E_{off} \right) \frac{v_c}{V_{ref}} i_c \quad (5)
\]

\[
P_{\text{SW,cont}}^{\text{Diode}} = \frac{1}{2\pi} \int E_{on} \frac{v_c}{V_{ref}} i_c \quad (6)
\]

IV. POWER LOSS DERIVATION FOR THE VSI+BC

The derivation of the power losses for the VSI+BC topology are performed in [7]. Therefore only the final results are presented here. Based on equation (1) and (2) the conducting losses shown in equations (7) and (8) are derived. They depend on the line current $i_L$ and the modulation index $M$ as well as on the power factor $\cos \varphi$.

\[
P_{\text{C,cont}}^{\text{IGBT}} = \frac{V_{CE,0} i_L}{2\pi} \left[ 1 + \frac{M\pi}{4} \cos(\varphi) \right] + \frac{r_{CE} i_L^2}{2\pi} \left( 1 + M \left( \frac{2}{3} \cos(\varphi) \right) \right) \quad (7)
\]

\[
P_{\text{C,cont}}^{\text{Diode}} = \frac{V_{F,0} i_L}{2\pi} \left[ 1 + \frac{M\pi}{4} \cos(\varphi) \right] + \frac{r_F i_L^2}{2\pi} \left( 1 + M \left( \frac{2}{3} \cos(\varphi) \right) \right) \quad (8)
\]

For calculating the switching losses for each semiconductor of the voltage source inverter equations (3) and (4) for the continuous PWM and (5) and (6) for the discontinuous PWM are adapted to the current and the voltage of the valve as presented in (9) and (10). The blocking voltage corresponds to the dc-link voltage $V_{DC}$ and the current to the peak line current $i_L$. The factor $N_{\text{cond/dic}}$ is 1 for the continuous and $\frac{1}{2}$ for the discontinuous modulation.

\[
P_{\text{SW,cont}}^{\text{IGBT}} = \frac{1}{\pi} \int \left( E_{on} + E_{off} \right) \frac{V_{DC}}{V_{ref}} i_L N_{\text{cond/dic}} \quad (9)
\]

\[
P_{\text{SW,cont}}^{\text{Diode}} = \frac{1}{\pi} \int E_{on} \frac{V_{DC}}{V_{ref}} i_L N_{\text{cond/dic}} \quad (10)
\]

The losses of the boost converter depend on the input current $i_0$ and the modulation index $\alpha$ that is defined as:

\[
\alpha = \frac{T_s}{T} = 1 - \frac{V_0}{V_{DC}} \quad (11)
\]

The modulation index is a function of the ratio of the input voltage to the output voltage that is in this case the
dc-link voltage. The IGBT of the boost converter is turned on for the time $T_{\text{on}}$.

The conducting losses are calculated by means of equation (12) and (13) for the IGBT and the diode, respectively.

$$P_{c,\text{IGBT}}^{\text{con}} = f_s \left( E_{\text{on}} + E_{\text{off}} \right) \frac{V_{\text{dc}}}{I_{\text{dc}}} \hat{i}_{\text{in}}$$  \hfill (12)

$$P_{c,\text{Diode}}^{\text{con}} = f_s \frac{V_{\text{dc}}}{I_{\text{dc}}} \hat{i}_{\text{in}}$$  \hfill (13)

The switching losses of the semiconductors of the boost converter are similar to the switching losses of the voltage source inverter, since the blocking voltage is also the dc-link voltage. The IGBT of the boost converter is short-circuited [1], [8] et al. In this case the switching frequency can be neglected.

V. Power Loss Derivation for the ZSI

A. Conducting Losses

While the input voltage is above $v_{\text{in}} > \sqrt{2} V_L$ the Z-source inverter operates like a VSI and the losses of the IGBTs and the freewheeling diodes are calculated like for the VSI (see above and [1]). However the smoothed dc-link current $i_{\text{in}}$ causes conducting losses within the dc diode $D_7$ [9]:

$$P_{c,\text{Diode}}^{\text{con}} = V_{\text{d}} \hat{i}_{\text{in}} + r_f \hat{i}_{\text{in}}^2$$  \hfill (16)

If the input voltage drops below $v_{\text{in}} < \sqrt{2} V_L$, another state, the so called shoot-through state is implemented to boost the input voltage [1] et al. During a shoot-through state all six IGBTs are conducting simultaneously and the dc-link is short-circuited [1], [8] et al.. In this case the current through one IGBT is the superimposition of the sinusoidal grid current and the high-frequency shoot-through current (see figure 3). In this sketch and for the calculations it is assumed that the line filter is large enough that the ripple of the line current caused by the switching frequency can be neglected.

For the calculation of the power losses both the mean value and the rms value are required and therefore a mathematical description of the waveform is needed.

The mean value is the sum of the mean values of half a fundamental period of the line current (17) and the shoot-through-current (18):

$$\bar{i}_l = \frac{P_{\text{VSI,21}}}{V_{\text{VSI,21}}} \left( \frac{2}{3} M \cos(\phi) \right)$$  \hfill (17)

$$\tilde{i}_s = \frac{P_{\text{VSI,21}}}{V_{\text{VSI,21}}} \left( \frac{2}{3} M \cos(\phi) \right)$$  \hfill (18)

M is the modulation index and D is the shoot-through-duty-cycle.

For the derivation of the rms of the current through one IGBT a mathematical description of the total waveform is required. But since the shoot-through-current is added discontinuously to the line current, a mathematical description is very difficult. For the following investigations an approximation is made: For small input voltages the rms of the shoot-through-current is much larger than that of the line current. In this case the deviation is acceptable small if just the rms of the shoot-through-current is derived and added to the average value of the line current. For higher input voltages the ratio of the shoot-through-current to the current through one IGBT decreases. In this case it is acceptable to add the rms of the line current to the mean value of the shoot-through-current. The decision if the input voltage is high or low is done by comparing $P_{c,\text{IGBT}}^{\text{con}}$, and $P_{c,\text{Diode}}^{\text{con}}$, which are the power losses for low and high input voltages. They are calculated in (19) and (20), respectively. If the value of equation (19) is greater than the value of (20) the input voltage is defined as low and equation (19) is applied and vice versa.

$$P_{c,\text{IGBT}}^{\text{con}} = V_{\text{d}} \left( \bar{i}_l + \bar{i}_s \right) + r_f \left( \hat{i}_l + \hat{i}_s \right)^2$$  \hfill (19)

$$P_{c,\text{Diode}}^{\text{con}} = V_{\text{d}} \left( \tilde{i}_l + \tilde{i}_s \right)$$  \hfill (20)

There $\bar{i}_l$ and $\bar{i}_s$ are the rms values of the shoot-through and the line current, which are calculated in equations (21) following [7] and (22), separately.

$$\bar{i}_l = \frac{P_{\text{VSI,21}}}{V_{\text{VSI,21}}} \left( \frac{\pi}{4} + \frac{M \frac{2}{3} \cos(\phi)}{2} \right)$$  \hfill (21)

$$\bar{i}_s = \frac{P_{\text{VSI,21}}}{V_{\text{VSI,21}}} \left( \frac{\pi}{4} - \frac{M \frac{2}{3} \cos(\phi)}{2} \right)$$  \hfill (22)

The freewheeling diodes only carry the grid current during the zero-states and are blocking during the shoot-through states. This leads to following conducting losses of one single diode [9]:

$$P_{c,\text{Diode}}^{\text{con}} = \left( \frac{V_{\text{d}} i_l}{2\pi} \left( 1 - M \frac{\pi}{4} \cos(\phi) \right) + \frac{r_f i_l^2}{2\pi} \left( 1 - M \frac{\frac{2}{3} \cos(\phi)}{2} \right) \right) \frac{\sqrt{3} M (3 - \pi)}{3\sqrt{3} M - 2\pi}$$  \hfill (23)

In all previous publications as far as the authors know the losses of the dc-diode $D_7$ are neglected. However the results developed here will show that these losses cannot be omitted. The diode is only blocking during the shoot-
through-states $T_0$. Figure 4 shows the simplified waveform of the current through the dc diode where the current transients due to switching occasions are unconsidered. The resulting deviation when calculating the conducting losses caused by this simplification is small because these transients amount to less than 1 percent of the total current and are on average zero, so that only the rms-value would be affected.

During the shoot-through-state the current flows through the inductances ($L_1$, $L_2$) and its stored energy increases as mentioned above. While the diode is conducting the current is limited by the inductances (L) which are connected in series. The current through the diode is sloping down due to the decreasing of the stored energy in the inductances. The waveform is described in (24) where $P_{in}$ is the input power:

$$i_{D7}(t) = \begin{cases} \frac{1}{2L} (V_n - V_C) (T - T_0) + \frac{P_{n} T}{V_n (T - T_0)} - \frac{2(V_n - V_C)}{L} t & 0 < t < \frac{T - T_0}{2} \\ 0 & \text{else} \end{cases}$$

This yield to the conducting losses of the dc-diode D7:

$$P_{con,D7} = P_{n} \frac{V_n}{V_r} + \tau_r \left[ \frac{P_{n} T}{V_n (T - T_0)} - \frac{1}{2L} (V_n - V_C)^2 \frac{T - T_0}{T} + \frac{1}{L} (V_n - V_C) \left( \frac{P_{n} T}{V_n (T - T_0)} + \frac{1}{2L} (V_n - V_C) \right) \left( \frac{T - T_0}{T} \right)^2 \right]$$

$$+ \frac{1}{3L} (V_n - V_C)^2 \left( \frac{T - T_0}{T} \right)^2$$

(25)

**B. Switching Losses**

The switching losses of all devices in the ZSI depend as for the VSI on the modulation method. If instead of the continuous the discontinuous modulation is used, the switching losses concerning the line current are halved in the same way as for VSI [11]. But also the losses evoked by the shoot-through-states are halved compared to the continuous PWM, because the number of zero-states and hence the number of shoot-through-states is halved as well but they appear twice as long. The following equations show the switching losses of one IGBT, one freewheeling diode and the dc diode separately. Again the factor $N_{con,dis}$ is one for the continuous and ½ for the discontinuous PWM.

$$P_{SW,DIS} = f_s \left( E_{on} + E_{off} \left( \frac{1}{\pi} \frac{\hat{V}_{on}}{V_{ref}} \frac{I_{ref}}{I_{ref}} + \frac{2P_{n}}{3V_{d,ref}} \right) \right) N_{con,dis}$$

(26)

$$P_{D,DIS} = \frac{1}{\pi} \frac{f_s}{V_{ref}} E_{on} \frac{\hat{V}_{on}}{V_{ref}} I_{ref} N_{con,dis}$$

(27)

$$P_{D7,DIS} = 2f_s E_{off} - V_c - V_0$$

$$\frac{P_{n}}{V_n} \frac{T}{T - T_0} - \frac{1}{2L} (V_n - V_C) (T - T_0)$$

(28)

The factor 2/3 in (26) arises because twice the dc-current is switched simultaneously in three phase legs.

**VI. DEFINITION OF EFFICIENCY, POWER SEMICONDUCTOR RATING**

Regarding losses and efficiency, only the influence of the power semiconductors is taken into account. The total losses of both topologies are the sum of the switching and conducting losses of all semiconductors as shown in (29) and (30).

$$P_{loss,BC} = 6(P_{SW,DIS} + P_{SW,BC} + P_{SW,DIS} + P_{SW,BC}) + P_{D,DIS} + P_{D,BC} + P_{D,BC}$$

(29)

$$P_{ZSI} = 6(P_{SW,DIS} + P_{SW,BC} + P_{SW,DIS} + P_{SW,BC}) + P_{D,DIS} + P_{D,BC}$$

(30)

The efficiency for the VSI+BC and for the ZSI is defined as following:

$$\eta_{VSI+BC} = 1 - \frac{P_{loss,BC}}{P_{in}}, \quad \eta_{ZSI} = 1 - \frac{P_{ZSI}}{P_{in}}$$

(31)

The costs for semiconductors are in a small power range nearly linear to their current carrying capability, as long as they have the same maximum blocking voltage and a similar loss performance [7]. The last point can be achieved by using the same type of semiconductors. To compare the VSI+BC and the ZSI topologies concerning their required semiconductor power, an installed semiconductor power has been established and defined as following for the IGBT, the free-wheeling and dc-diode, separately:

$$P_{SW,DIS} = V_{ces} I_c, \quad P_{D,DIS} = V_{ces} I_F$$

(32)

$I_c$ is the rated dc collector current of the IGBTs, $I_F$ the maximum dc forward current of the diodes and $V_{ces}$ is the maximum blocking voltage according to the datasheets.

**VII. METHOD OF SIMULATION**

The intention of this paper is to present a comparison of the VSI+BC and ZSI for different dc input voltages and a constant three phase 50 Hz output voltage that is
chosen to 400 V line to line. At the same time every single semiconductor both in IGBTs and (freewheeling-) diodes is chosen as small as possible for any operating point. Because the maximum permitted junction temperature is the limiting factor for the choice of size of the devices, the junction temperature is calculated for all semiconductors and working points separately. The size of the devices is chosen according to the maximum value of the datasheet thus the junction temperature is \( T_{JC} = 125^\circ C \) at a case temperature of \( T_c = 80^\circ C \). The stationary relationship between junction temperature and power losses is given by equation (33) where \( R_{th,J} \) is the thermal resistance between junction and case.

\[
T_J = R_{th,J} (P_J + P_C) + T_C
\]  

(33)

The dimension of the power semiconductors by their junction temperature can lead to (theoretical) fractional numbers of power semiconductors or rather sizes that are not available on the market. Therefore it is necessary to interpolate between the relevant data given in Table I and II which are based on [12][13].

VIII. COMPARABILITY OF ZSI AND VSI+BC CONCERNING LOSSES AND INSTALLED POWER

Since the operating principles of the ZSI and VSI+BC are very different, a global comparison is difficult. The main issue is that both the VSI and the dc-dc converter work well with 1200 V IGBTs and diodes. However the ZSI requires 1700 V modules for input voltages less than 400 V [8]. The reason therefore is that peak voltage across the IGBT’s \( \hat{v}_{dc} \) increases with small input voltages as shown in equation (34) [8].

\[
\hat{v}_{dc} = \frac{V_v}{\sqrt{3M-1}} \quad \text{with} \quad M = \frac{2\sqrt{2V_{av}}}{V_{str}}
\]  

(34)

Figure 5 shows the maximum voltage across the IGBT’s depending on the input voltage and neglecting overshoots caused by stray inductances. Characteristic of the high-voltage devices is that they feature incomparable threshold voltages, differential resistances and thermal resistances of the IGBT’s as shown in Table I and II. That is why the results for both topologies are presented with 1200 V and 1700 V IGBTs and diodes. For all results an input power of 20 kW and cos(\( \phi \))=1 is assumed. At an input voltage exceeding 575 V both inverters operate as VSIs. That means that the IGBT of the boost converter is conducting continuously and that the ZSI stops providing any shoot-through state. For all calculations it is supposed that the dc link voltages and currents are ideal and without any ripple. All results are presented for the continuous and discontinuous PWM since the switching losses of the ZSI have been emphasized as the major losses and thus can be reduced by the discontinuous PWM.

IX. COMPARISON OF LOSSES, EFFICIENCY AND INSTALLED SEMICONDUCTOR POWER

Figures 6 and 7 show the efficiency of both topologies for the continuous and discontinuous PWM. The green dotted line describes unrealizable working points of the ZSI with 1200 V IGBTs. It can be seen that the VSI+BC topology (black dotted line) has a better

\[\text{Figure 5. Voltage across the IGBT's of the ZSI vs. input dc voltage for a grid voltage of 400 V}\]
performance for almost every input voltage. Only for an input voltage around 500 V the ZSI is topping its counterpart by using the discontinuous PWM and ensuring a minimum input voltage of 400 V (solid green line). Especially for low input voltages the performance of the ZSI is worse because of the opposed behavior by achieving a high voltage gain by extending the shoot-through-states and consequently as well extending the zero states which have a buck effect. That results in high voltages across the semiconductors and large current through the IGBT’s during the shoot-through states.

The reason for the different behavior of the topologies is on the one hand that the VCI of the VCI+BC system works with a modulation index of M=1 and has consequently only a small buck behavior compared to the ZSI. There the length of the shoot-through-states and consequently as well the duration of the zero-states have to be extended for low input voltages.

On the other hand there is the disadvantage of only one transistor (the one of the boost converter) in the VSI+BC that has to cope with the shoot-through current compared to six transistors within the ZSI.

That leads to the rated semiconductor power that is presented in figures 8 and 9 for a continuous and for a discontinuous PWM. Again the VSI+BC system with 1200 V semiconductors has the best performance in all operating points. That means that this topology needs the least amount of silicon. For a ZSI working in the full input voltage range three and five times as much installed semiconductor power for the discontinuous and continuous PWM is required respectively. The reason for that is again the buck behavior of the inverter of the ZSI where long shoot-through-states are required. That causes very high voltages across the power semiconductors and very large current through six devices instead of one for the VSI+BC inverter.

Nevertheless the power losses of the passive components are disregarded. However a close look at the waveforms of the current through the inductances and capacitors of both the topologies points to the fact that the power losses of the passive elements of the ZSI are clearly higher than for VSI+BC.

However these results are only valid for the 400 V grid. The curves may look somewhat different for lower grid voltages.

X. CONCLUSION

In wind power stations there are converter configurations where the generator current is rectified by diodes. The resulting voltage depends on the variable rotor speed of the wind turbine and has to be boosted and inverted to feed power to the grid. The Z-source inverter is a new solution for this task. Here its power losses, efficiency and installed semiconductor power are compared to the conventional solution with voltage source inverter linked with a dc/dc boost converter.

This is done by calculating the rms of the current through the IGBT’s of the Z-source inverter. Based on the mean and rms values of current and voltage of the valves the power losses of all semiconductors are calculated for the ZSI as well as for the voltage source inverter linked with dc/dc boost converter. Since these two topologies have the same input and output...
characteristics they have been compared to each other concerning their power losses of the semiconductors, their efficiency and their rated power.

The results show that the power losses of the semiconductors of the Z-source inverter are significant higher than for the VSI+BC topology although the ZSI has one device less. Because of that also the efficiency of the ZSI is worse compared to the VSI+BC system. To achieve a high voltages gain by applying long shoot-through-states a lot of semiconductor power is required because the buck converting zero states have to be extended at the same time. It is also shown that the PWM method has higher influences on the losses of the ZSI compared to the VSI+BC since the switching losses are dominating the total semiconductor losses of the ZSI.

REFERENCES


