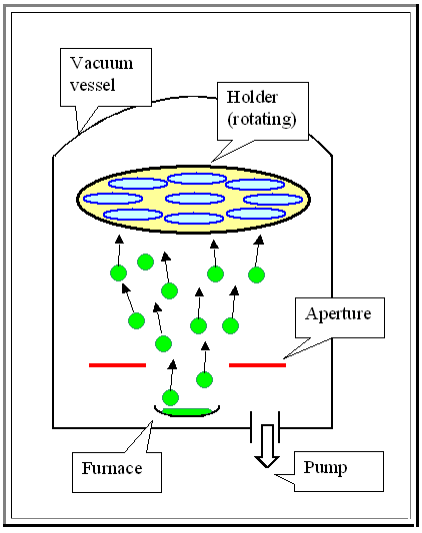
6.3.3 Miscellaneous Techniques and Comparison

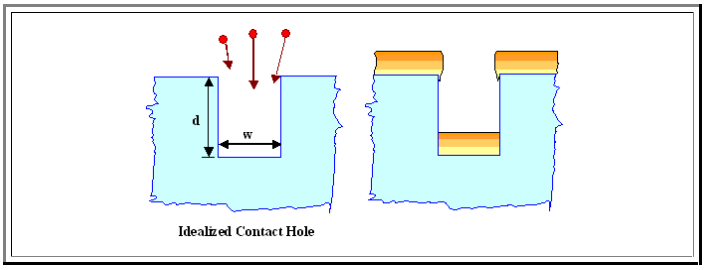
Evaporation

- By now you may have wondered why the time-honored and widely used technique of evaporation has not been mentioned in context with **Si** technology.
  - The answer is simple: *It is practically not used*. This is in contrast to other technologies, notably optics, where evaporation techniques played a major role.
  - In consequence, this paragraph shall be kept extremely short. It mainly serves to teach you that there are more deposition techniques than meets the eye (while looking at a chip).
- What is the evaporation technique? If your eye glasses or your windshield ever fogged, you have seen it: Vapor condenses on a cold substrate.



- What works with water vapor also works with all other vapors, especially metal vapor.
- All you have to do is to create the vapor of your choice, always inside a vacuum vessel kept at a good vacuum. The (usually) metal atoms will leave the crucible or "boat" with an kinetic energy of a few **eV** and sooner or later will condense on the (cooled) substrate (and everywhere else if you don't take special precautions).
- Your substrate holder tends to be big, so you can accommodate several wafers at once (Opening up and loading vacuum vessels takes expensive time!)

- The technique is relatively simple (even taking into account that the heating nowadays is routinely done with high power electron beams hitting the material to be evaporated), but has major problems with respect to **IC** production:
  - The atoms are coming from a "point source", i.e. their incidence on the substrate is nearly perpendicular. Our typical contact hole filling problem thus looks like this:



  - In other words: Forget it!
  - It is also clear that it is very difficult to outright impossible to produce layers with arbitrary composition, e.g. **Al** with **0,3% Si** and **0,5% Cu**. You would need three independently operated furnaces to produce the right mix.
- All things considered, sputtering is usually better and evaporation is rarely used nowadays for microelectronics.

Spin-on Techniques

- **Spin-on techniques**, a special variant of so-called *sol-gel techniques*, start with a liquid (and usually rather viscous) source material, that is "painted" on the substrate and subsequently solidified to the material you want.

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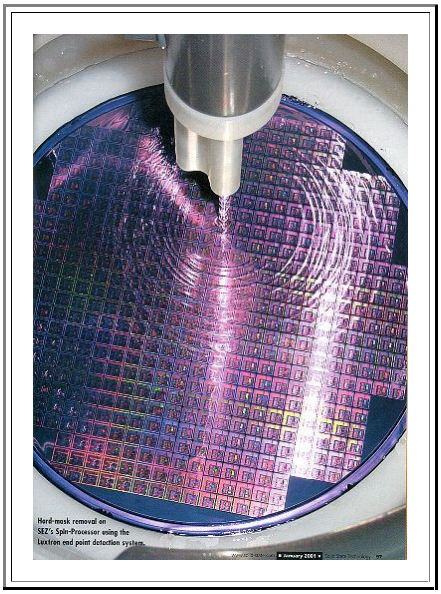
- The "*painting*" is not done with a brush (although this would be possible), but by spinning the wafer with some specified **rpm** value (typically **5000 rpm**) and dripping some of the liquid on the center of the wafer. Centrifugal forces will distribute the liquid evenly on the wafer and a thin layer (typically around **0,5 µm**) is formed.
- Solidification may occur as with regular paint: the solvent simply evaporates with time. This process might be accelerated by some heating. Alternatively, some chemical reaction might be induced in air, again helped along by some "baking" as it is called.



- As a result you obtain a thin layer that is rather smooth - nooks and crannies of the substrate are now planarized to some extent. The film thickness can be precisely controlled by the angular velocity of the spin process (as a function of the temperature dependent viscosity of the liquid).
  - Spin-on coating is the technique of choice for producing the light-sensitive **photo resist** necessary for lithography. The liquid resist rather resembles some viscous paint, and the process works very well. It is illustrated on the right.
  - Most other materials do not have suitable liquid precursors, the spin-on technique thus can not be used.

- A noteworthy exception, however, is **spin-on glass**, a form of **SiO_2** mentioned before.
  - The liquid consists basically of Silicon-tetra-acetate (**$Si(CH_2COOH)_4$**) (and some secret additions) dissolved in a solvent. It will solidify to an electronically not-so-good **SiO_2** layer around **200 ^oC**.
  - Using spin-on glass is about the only way to fill the interstices between the **Al** lines with a dielectric at low temperatures. The technique thus has been developed to an art, but is rather problematic. The layers tend to crack (due to shrinkage during solidifications), do not adhere very well, and may interact detrimentally with subsequent layers.
- A noteworthy example of a material that can be "spun on", but nevertheless did not make it so far are **Polyimides**, i.e. polymers that can "take" relatively high temperatures
  - They look like they could be great materials for the intermetal dielectric - low ϵ_r, easy deposition, some planarizing intrinsic to spin-on, etc. They are great materials - but still not in use. If you want to find out why, and how new materials are developed in the real world out there, use this link.

Other Methods

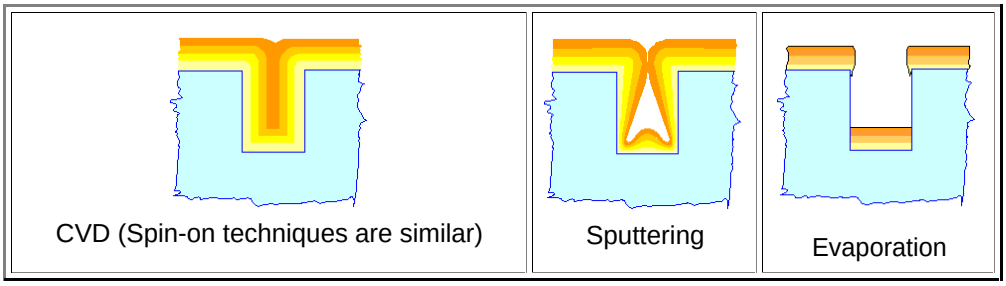
- Deposition techniques for thin layers is a rapidly evolving field; new methods are introduced all the time. In the following a couple of other techniques are listed with a few remarks
- **Molecular Beam Epitaxy** (***MBE***). Not unlike evaporation, except that only a few atoms (or molecules) are released from a tricky source (an "effusion cell") at a time.
  - **MBE** needs ultra-high vacuum conditions - i.e. it is very expensive and not used in **Si-IC** manufacture. **MBE** can be used to deposit single layers of atoms or molecules, and it is relatively easy to produce multi layer structures in the **1 nm** region. An example of a **Si-Ge** multilayer structure is shown in the link
  - **MBE** is the method of choice for producing complicated epitaxial layer systems with different materials as needed, e.g., in advanced optoelectronics or for superconducting devices. An example of what you can produce with **MBE** is shown in the link
- **Laser Ablation**. Not unlike sputtering, except that the atoms of the target are released by hitting it with an intense Laser beam instead of **Ar** ions extracted from a Plasma.
  - Used for "sputtering" ceramics or other non conducting materials which cannot be easily sputtered in the conventional way.
- **Bonding techniques**. If you bring two ultraflat **Si** wafers into intimate contact without any particles in between, they will just stick together. With a bit of annealing, they fuse completely and become bonded.
  - Glass blowers have done it in a crude way all the time. And of course, in air you do not bond **Si** to **Si**, but **SiO_2** to **SiO_2**. One way to use this for applications is to produce a defined **SiO_2** layer first, bond the oxidized wafer to a **Si** wafer, then polish off almost all of the **Si** except for a layer about **1 µm** thick
  - Now you have a regular wafer coated with a thin oxide and a perfect single crystalline **Si** layer - a so-called "**silicon on insulator**" (***SOI***) structure. The **Si** industry in principle would love **SOI** wafers - all you have to do to become rich immediately, is to make the process cheap. But that will not be easy. You may want to check why **SOI** is a hot topic, and how a major company is using wafer bonding plus some more neat tricks, including mystifying electrochemistry, to make **SOI** affordable.

- Bonding techniques are rather new; it remains to be seen if they will conquer a niche in the layer deposition market.

- **Galvanic techniques**, i.e. electrochemical deposition of mostly metals. Galvanizing materials is an old technique (think of chromium plated metal, anodized aluminium, etc.) normally used for relatively thick layers.
  - It is a "dirty" process, hard to control, and still counted among the black arts in materials science. No self-respecting **Si** process engineer would even dream of using galvanic techniques - except that with the advent of **Cu** metallization he was not given a choice.
  - Using **Cu** instead of **Al** for chip metallization was unavoidable for chips hitting the market around **1998** and later - the resistivity of the **Al** was too high.
  - As it turned out, established techniques are no good for **Cu** deposition - galvanic deposition is the method of choice. **Cu** metallization calls for techniques completely different from Al metallization - the catchword is "damascene technology". The link takes you there - you may also enjoy this module from the *"Defects" Hyperscript* because it contains some other interesting stuff in the context of (old) materials science.
- And not to forget: Galvanic techniques are also used in the packaging of chips

Comparison of Various Layer Deposition processes

- *First*, lets look at **edge coverage**, i.e. the dependence on layer thickness on the topography of the substrate. This is best compared by looking at the ability to fill a small contact hole with the layer to be deposited.
  - We have the following schematic behavior of the major methods as shown before.



- *Second*, lets look at what you can deposit.
  - **CVD** methods are limited to materials with suitable gaseous precursors. While it is not impossible to deposit mixtures of materials (as done, e.g. with doped poly **Si** or flow glass), it will not generally work for arbitrary compositions.
  - Sputter methods in practice are limited to conducting materials - metals, semiconductors, and the like. Arbitrary mixtures can be deposited; all you have to do is make a suitable target. The target does not even have to be homogeneous; you may simply assemble it by arranging pie-shaped wedges of the necessary materials in the required composition into a "cake" target.
  - Evaporation needs materials that can be melted and vaporized. Many compounds would decompose, and some materials simply do not melt (try it with **C**, e.g.). If you start with a mixture, you get some kind of distillation - you are only going to deposit the material with the highest vapor pressure. Mixtures thus are difficult and can only be produced by co-evaporation from different sources.