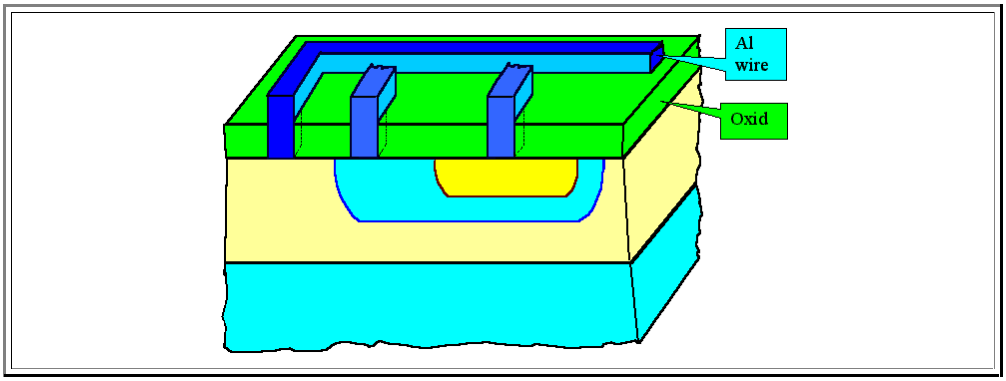
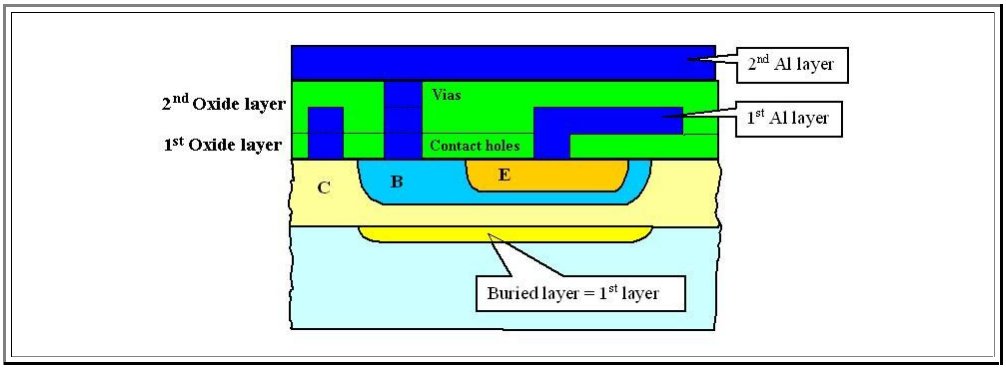
5.1.3 Basic Concepts of Connecting Transistors

- How do we connect a few million transistors - i.e. run signal wires from transistor **x** to transistor **y** (**x** and **y** being arbitrary integers between **1** and about **50 000 000**?) and connect *all* transistors to some voltage and current supply - and all that *without wires crossing*?
  - For state-of-the-art **ICs** this is one of the bigger challenges. Obviously you must have wiring on several planes because you cannot avoid that connections must cross each other.
  - The first level is simple enough - in principle! Lets see this in a schematic drawing.



- So all you do is to cover everything with an insulator. For that you are going to use **SiO_2**, which is not only one of the best insulators there is, but is easily produced and fully compatible with **Si**.
  - On top of this oxide you now run your "wires" from here to there, and wherever you want to make a contact to a transistor, you make a **contact hole** in the **SiO_2** layer.
  - Every transistor needs three contact holes - and as you can see in the drawing, you rather quickly run into the problem of crossing connections.
- What we need is a **multi-level metallization**, and how to do this is one of the bigger challenges in integration technology.
  - Fortunately, we already have a second level in the **Si** - it is the "**buried layer**" that we put down before adding the epitaxial layer. It can be structured to connect the collectors of all transistors where this makes sense. And since the collectors are often simply connected to the power supply, this makes sense for most of the transistors.
  - But this is not good enough. We still need more metallization layers on top. So we repeat the "putting oxide down, making contact holes, ..etc". procedure and produce an second metallization layer:



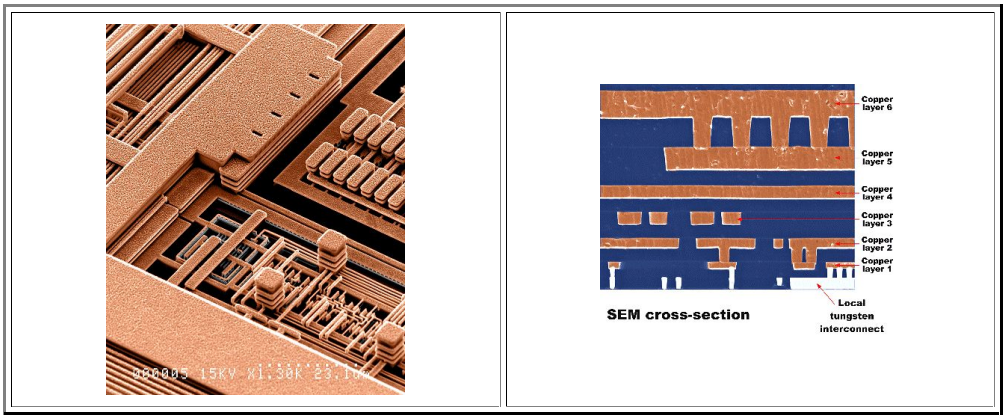
- If you get the idea that this is becoming a trifle complicated, you get the right idea. And you haven't seen anything yet!
  - State-of-the-art **ICs** may contain **7** or more connection (or metallization) layers. For tricky reasons explained later, besides Aluminium (**Al**), Tungsten (**W**) is employed, too, and lately **Al** is being replaced by Copper (**Cu**).
  - Between the metal layers we obviously need an "**intermetal dielectric**". We could (and do) use **SiO_2**; but for modern chips we would rather use something better. In particular, a material with a smaller dielectric constant (**SiO_2** has a value of about **3.7**). Polymers would be fine, in particular polyimides, a polymer class that can "take the heat", i.e. survives at relatively high temperatures. Why we do not have polyimides in use just now is an interesting story that can serve as a prime example of what it means to introduce a new material into an existing product.
- Why are we doing this - replacing trusty old **Al** by tricky new **Cu** - at considerable costs running in the billion **$** range?
  - Because the total resistance ***R*** of an **Al** line is determined by the specific resistivity **ρ = 2,7 $\mu\Omega$cm** of **Al** and the geometry of the line. Since the dimensions are always as small as you can make it, you are stuck with **ρ**.

- Between neighbouring lines, you have a parasitic capacitance ***C***, which again is determined by the geometry and the dielectric constant ϵ of the insulator between the lines. Together, a **time constant** $R \cdot C$ results, which is directly proportional to $\rho \cdot \epsilon$. This time constant of the wiring - found to be in the **ps** region - gives an absolute upper limit for signal propagation. If you don't see the probem right away, turn to this basic module.
- In other words: Signal delay in **Al** metallization layers insulated by **SiO_2** restricts the operating frequency of an **IC** to about **1 GHz** or so.

This was no problem before **1998** or so, because the transistors were far slower anyway. But it is a problem *now* (**2000 +**)!

- Obviously, we must use materials with lower ρ and ϵ values. Choices are limited, however - **Cu (ρ = 1,7 μΩcm)** is one option that has been chosen; the last word about a suitable replacement for **SiO_2** (having ϵ **= 3,7**) is not yet in.

Here are famous pictures of an advanced **IBM** chip with **7** metallization layers, completely done in **W** and **Cu**. In the picture on the left, the dielectric between the metals has been etched off, so only the metal layers remain.



The transistors are not visible at this magnification - they are too small. You would find them right below the small "local tungsten interconnects" in the cross sectional view.

Before we go into how one actually does the processes mentioned (putting down layers, making little contact holes, ...), we have to look at how you make *MOS transistors* as opposed to *bipolar* transistors. We will do that in the next sub-chapter.