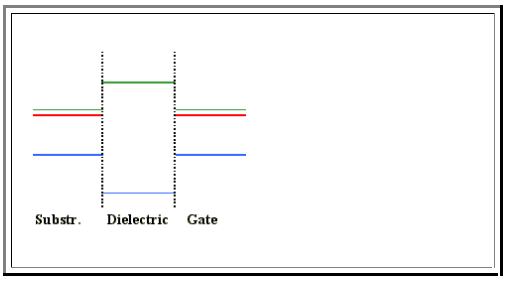
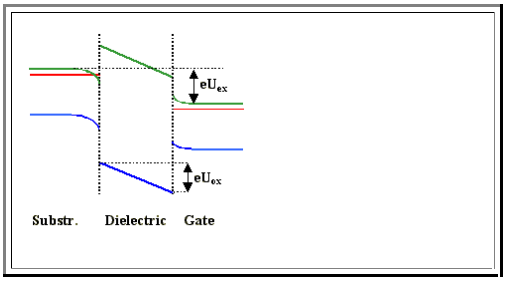
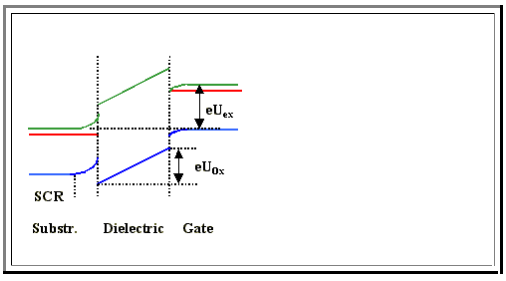
Der MOS Transistor mehr quantitativ

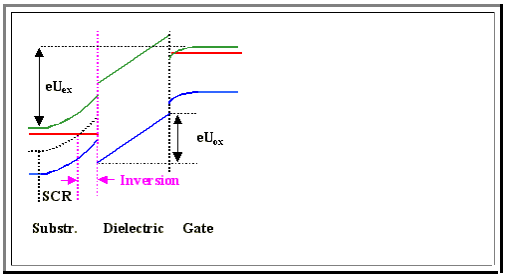
Advanced

Some Quantitative Considerations

The decisive part is achieving *inversion*. Lets see how that looks like in a band diagram. To make life easier, we make the gate electrode from the same kind of **n-Si** as the substrate, just highly doped so it is as metallic as possible - we have the same kind of band diagram then to the left and right of the gate dielectric

Lets look schematically what that will give us for some basic cases:

Voltage at the gate	Conditions in the Si	Voltage drop	Charge distribution
Zero gate voltage. "**Flat band**" condition 	Nothing happens. The band in the substrate is perfectly flat (and so is the band in the contact electrode, but that is of no interest).	We only would have a voltage (or better potential) drop, if the Fermi energies of substrate and gate electrode were different	There are no *net* charges
Pos. gate voltage. **Accumulation** 	With a positive voltage at the gate we attract the electrons in the substrate. The bands must bend down somewhat, and we increase the number of electrons in the conduction band accordingly. (There is a bit of a space charge region (SCR) in the contact, but that is of no interest).	The voltage drops mostly in the oxide	There is some *pos. charge* at the gate electrode interface (with our **Si** electrode from the **SCR**), and *negative charge* from the many electrons in the (thin) accumulation layer on the other side of the gate dielectric.
Small neg. gate voltage. **Depletion** 	With a (small) negative voltage at the gate, we repel the electrons in the substrate. Their concentration decreases, the hole concentration is still low - we have a layer depleted of mobile carriers and therefore a **SCR**.	The voltage drops mostly in the oxide, but also to some extent in the **SCR**.	There is some *negative charge* at the gate electrode interface (accumulated electrons with our **Si** electrode), and *positive charge* smeared out in the the (extended) **SCR** layer on the other side of the gate dielectric.
Large neg. gate voltage. **Inversion**			



With a (large) negative voltage at the gate, we repel the electrons in the substrate very much. The bands bend so much, that the Fermi energy (red line) is in the lower half of the band close to the interface. In this region holes are the majority carriers, we have *inversion*. We still have a **SCR**, too.

The voltage drops mostly in the oxide, but also to some extent in the SCR and the inversion layer.

There is more *negative charge* at the gate electrode interface (accumulated electrons with our **Si** electrode), some *positive charge* smeared out in the the (extended) **SCR** layer on the other side of the gate dielectric, and a lot of *positive charge* from the holes in thin inversion layer.

- Qualitatively, this is clear. What happens if we replace the (highly **n**-doped) **Si** of the gate electrode with some metal (or **p**-doped **Si**)?
  - Then we have *different Fermi energies* to the left and right of the contact, leading to a *built-in potential* as in a **pn**-junction. We will than have some band bending at zero external voltage, flat band conditions for a non-zero external voltage, and concomitant adjustments in the charges on both sides.
  - But while this complicates the situation, as do unavoidable fixed immobile charges in the dielectric or in the **Si**-dielectric interface, nothing new is added.
- Now, the decisive part is achieving inversion. It is clear that this needs some minimum threshold voltage U_{th}, and from the pictures above, it is also clear that this request translates into a request for some *minimum charge* on the capacitor formed by the gate electrode, the dielectric and the **Si** substrate.
  - What determines the amount of charge we have in this system? Well, since the whole assembly for any distribution of the charge can always be treated as a simple capacitor C_G, we have for the charge of this capacitor, .

$$Q_G = C_G \cdot U_G$$

  - Since we want U_{th} to be small, we want a *large gate capacitance* for a large charge Q_G, and now we must ask: What determines C_G?
- If all charges would be concentrated right at the interfaces, the capacitance *per area unit* would be given simply by the geometry of the resultant plate capacitor to

$$C_G = \frac{\epsilon\epsilon_0}{d_{Ox}}$$

  - With d_{Ox} = thickness of the gate dielectric, (so far) always silicon dioxide SiO_2.
- Since our charges are somewhat spread out in the substrate (we may neglect this in the gate electrode if we use metals or very highly doped **Si**), we must take this into account.
  - In electrical terms, we simply have a second capacitor C_{Si} describing the effects of spread charges in the Si, switched in series to the geometric capacitor which we now call **oxide capacitance** C_{Ox}. It will be rather large for concentrated charges, i.e. for accumulation and inversion and small for depletion.
  - The total capacitance C_G then is given by

$$\frac{1}{C_G} = \frac{1}{C_{Ox}} + \frac{1}{C_{Si}}$$

- For inversion and accumulation, when the most of the charge is close to the interface, the total capacitance will be dominated by C_{Ox}. It is relatively large, because the thickness of the capacitor is small.
  - In the depletion range, C_{Si} will be largest and the total capacitance reaches a minimum.
  - In total, C_G as a function of the voltage, i.e. $C_G(U)$ runs from a constant value at large positive voltages through a minimum back to about the same constant value at large positive voltages. The resulting curve contains all relevant information about the system. Measuring $C_G(U)$ is thus the first thing you do when working with **MOS** contacts.

- While it is not extremely easy to calculate the capacitance values and everything else that goes with it, it can be done - just solve the Poisson equation for the problem.

All things considered, we want C_{Ox} to be *large*, and that means we want the dielectric to be *thin* and to have a *large* dielectric constant - as stated above without justification.

- We also want the dielectric to have a large breakdown field strength, no fixed charges in the volume, no interface charges, a very small **tg δ**; it also should be very stable, compatible with **Si** technology, and cheap.
- In other words, we wanted**SiO_2** - even so its dielectric constant is just a mediocre **3.9** - for all those years of microelectronic wonders. But now (**2001**), we want something better with respect to dielectric constants. Much work is done, investigating, e.g., **CeO_2**, **Gd_2O_3**, **ZrO_2**, **Y_2O_3**, **$BaTiO_3$**, **BaO/SrO**, and so on. And nobody knows today (**2002**) which material will make the race!

- In **2007** we know more: It's **HfO_2**; at least for Intel. For reasons of it's own, Intel talks about Hafnium "metal", which makes no sense whatsoever