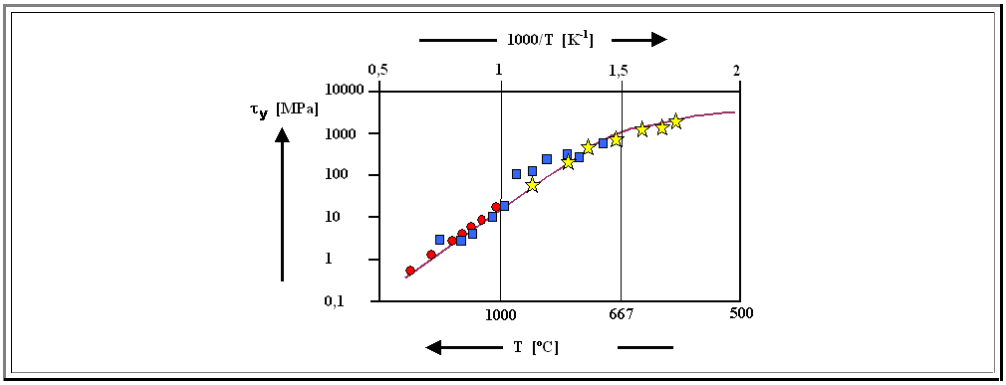
3.1.3 Mechanical, Thermal, and Other Properties

Mechanical Properties

- Silicon at *room temperature* is brittle - and that is about all there is to know.
- Well not quite. *First* of all, fracture of **Si** is quite an interesting topic to many people (searching for "fracture+silicon" produces about **20.000** hits in the Net)
  - *Second*, there is brittle, and there is *very* brittle. What is the case for **Si**? While the microelectronics industry has learned not to break its wafers (that's the main reason why they are so thick), the crystalline **Si** (or ***Si-c***) solar cell industry cannot afford to waste **Si** and keeps its "multi-crystalline" **(10 × 10)cm^2** slices as thin as possible (about **300 µm**). As a result, breakage of the slices is becoming the major problem in industrial solar cell production. At present (**2001**) large research projects are started to find out more about fracture of (multicrystalline) **Si**.
  - Fracture toughness, to give some numbers, has been reported to be **1.19 MPa · m^{½}** for the **{100}** tensile surface and **1,05 MPa · m^{½}** for the **{111}** tensile surface - there are certainly other numbers out there, too.
  - If we compare that to, e.g., the fracture toughness of *Steel* (≈ **200 MPa · m^{½}**), *Nylon* (≈ **3 MPa · m^{½}**), or ceramics like *Silicon nitride* (**Si_3N_4**, *Silicon carbide* (**SiC**) or *Alumina* (**Al_2O_3**) which are all ≈ **(3 - 5) MPa · m^{½}**, or common *glass* (≈ **0,8 MPa · m^{½}**), we see that **Si** is about as brittle as glass and "more" brittle than some of the tougher ceramics.
- Then we have the emerging "MEMS" industry, i.e **Micro Electronic and Mechanical Systems**. Obviously, the mechanical properties, especially the elastic coefficients and the elastic moduli are of prime interest (besides fracture, which simply must be avoided).
  - Youngs modulus, is given as **131 GPa** (or **107 GPa**, or ...; it depends on the source), which again should be compared to that of *diamond* (**1 000 GPa**, the biggest there is), *"hard" steels* (≈ **200 GPa**), *ceramics* (as above; ≈ **400 GPa**), *Silver* and *gold* (≈ **80 GPa**), or *Nylon* (≈ **3 GPa**).
  - All in all, Silicons elastic properties are pretty good, but not breathtaking.
- But let's not forget that in most processes we heat up the **Si** to temperatures somewhere between **700 °C** and **1200 °C**, and at high temperatures **Si** is no longer brittle but **ductile**, i.e. it deforms plastically.
  - Plastic deformation is always characterized by the **yield stress τ_y** which describes macroscopically the minimum shear stress needed to induce *plastic deformation*, and microscopically the minimum stress needed to induce *dislocation movement*.
  - In a somewhat simple minded approach, we see that **Si** is brittle and fractures if the yield stress **τ_y** is larger than the stress needed for facture under the conditions used. Since the yield stress decreases with increasing temperature, we expect that plastic deformation takes over at some temperature.
  - The figure below gives a compilation of **τ_y** data for **Si** (from a paper by J. Rabier and J.L. Demenet; phys stat sol (b) 222, 63 (2000)).



- In short, you must expect plastic deformation if the temperature is above, say **700 °C** and you have some stress acting on your **Si**.
  - If you started with a typical, completely dislocation free wafer, the initial **τ_y** might be somewhat larger because you first must generate some dislocations (which then can multiply).
  - If some dislocations have been generated, however, its all over. You will experience plastic deformation and you will have introduced dislocations irreversibly into your material.
- Where do stresses come from? There are *two* major sources:

- **1.** Running a batch of **Si** wafers (or slices, or whatever) into a piece of equipment that heats up the **Si**, the outside of the wafer will always tend to be hotter than the inside during heating up, and vice verse during cooling down. Thermal expansion will be different in different parts of the specimen, and that introduces stresses directly proportional to the *temperature gradient* in the sample. There is nothing you can do except keep the temperature gradients below the critical level. Typical tricks are to move into some oven s l o w l y , to have the equipment at some lower temperature and then go up slowly after the **Si** is inside, or to do both.
- **2.** If there are any layers on the **Si** (or inside, e.g. heavily doped regions), differences in thermal expansion coefficients will generate stresses at sometimes very large levels. Again, while you cannot avoid the stress produced by the layer you need, you can use some tricks to minimize the over-all stresses: Keep the area small (provide holes in the layer where it is not needed); put the same kind of layer on the backside - the combined effects cancel to some degree, and be generally aware of what you have on the backside (many layers are automatically also deposited on the backside, and there are good and not so good times in a process sequence when you can take them off).

If everything fails, you may want to try out some **Si** with a relatively high concentration of interstitial oxygen, $\mathbf{O_i}$ (say around **20 ppm**).

- These impurity atoms make dislocation movement more difficult (and thus increase τ_y) without degrading electronic properties too much (if you are lucky).

Last not least we note that the exact process of dislocation generation and movement, with particular respect to the details of the dislocation fine structure, is of major interest to basic research, since ultra-perfect **Si** is an ideal proving ground for theories concerning deformation and dislocations in covalently bonded crystals.

Thermal Properties

The most important thermal properties of Silicon are:

- **Thermal expansion coefficient** α_T,
- **Thermal conductivity k**, and, to a lesser extent
- **Specific heat** $\mathbf{c_p}$

The *thermal expansion coefficient* is crucial whenever other materials are in contact with **Si**, or if temperature gradients are encountered. In both cases it is rather easy to destroy the device by building up large mechanical stresses leading to fracture or plastic deformation. Lets see why

- **Si** is in contact with other materials *either* during processing (when, e.g., a layer of $\mathbf{SiO_2}$ or $\mathbf{Si_3N_4}$ or **Al** or ..., is deposited, often on the front *and* backside, *or*, as a finished device, when it is encapsulated in some housing, i.e. when it is packaged.

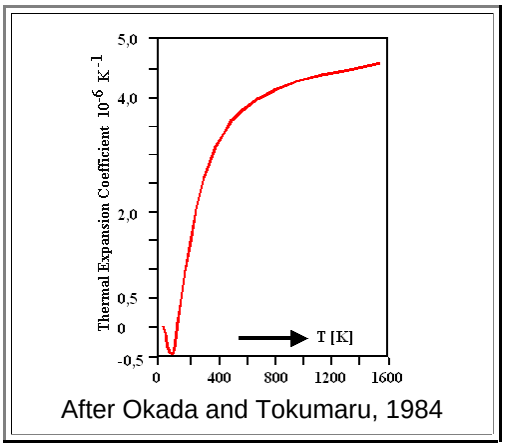
If temperature changes for a **Si** / other material *compound* - because you use your cellular phone during skiing and in the summer, or because processing the wafer intrinsically needs high temperature - mechanical stress, being roughly proportional to the difference in thermal expansion coefficients and the amount of material present, is simply *unavoidable*.

- The art of processing and packaging thus includes to keep the stress levels *always* below the critical stresses required to induce plastic deformation or fracture. You may have to optimize the thermal expansion coefficient of materials in contact with **Si** - if you can.
- The black polymer compound, for example, that is universally used for cheap packaging, while still very different in thermal expansion, is matched as much as possible. Since this is still not good enough, the **Si** chips are usually ground down to a thickness far below the original wafer thickness.

As we have seen above. if there is a *temperature gradient* in a piece of pure **Si** (e.g. a wafer), the hotter parts want to expand more then the cooler parts - again a mechanical stress is induced that is proportional to the temperature gradient *and* the thermal expansion coefficient.

- This is why you heat up the wafers s l o w l y, giving enough time for temperature equilibration. Otherwise, plastic deformation will occur, ruining your chips and leaving a wafer that is no longer flat - wafer **warpage**, one of the absolutely deadly wafer diseases, has occurred

Here are data of the *linear* (as opposed to "*volume*") thermal expansion of **Si** and some comparison to other relevant materials



After Okada and Tokumaru, 1984

- At low temperatures, α_T shows a pronounced minimum; an effect not easy to understand in cubic crystals, but nevertheless observed in most of the other cubic semiconductors, too. If we take the room temperature value of about **2,5 · 10^{-6} K^{-1}**, and compare it to the values of other materials important in **Si** technology, we have

Material	Si	Ge	GaAs	SiO_2	Si_3N_4	Al	Polymers
α_T [10^{-6} K^{-1}]	2,5	5,8	6,86	0,5	3,2	24	ca. 50 ... 200

The *thermal conductivity* κ is important, because **Si** chips, like most semiconductor devices, are producing lots of heat in operation. It must transported out of the system and the resistance to heat flow is given by the thermal conductivity of the material.

- What do we have? Here is the **Si** value, again together with thermal conductivities of other relevant materials. Note that κ is strongly temperature and structure dependend. For **Si_3N_4**, as an example, values may scatter from **0,2 - 1,2 W·cm^{-1} · K^{-1}** .

Material	Si	Ge	GaAs	SiO_2	Si_3N_4	SiC	Diamond	Cu; Ag
κ [W · cm^{-1} · K^{-1}] at room temperature	1,5 1,4	0,6	0,46 0,54	ca. 0,014	ca. 0,2	ca. 3.5 (3 - 5)	ca. 10 - 30	4

- **Diamond**, surprisingly, is the champion - and that is why thin diamond layers are sometimes used to transport the heat generated in some device to some heat sink as efficiently as possible.

While it appears that you just must live with whatever thermal conductivity a material has - this is not entirely true. The thermal conductivity can be made substantially better, if the material is made from *one isotope only*!

- Here is a recent (may **2002**) topic form the news ticker in the semiconductor business.

Isonics Delivers Silicon-28 SOI Wafers
Online staff -- 5/2/2002
Electronic News

Isonics Corp. of Golden, Colo., today said that a major semiconductor manufacturer has taken delivery of Silicon-28 silicon-on-insulator (SOI) wafers for evaluation.
Isotopically purified silicon-28 has 60 percent more thermal conductivity than natural silicon, Isonics said. This allows for reductions in the self heating of circuits made with natural SOI wafers. Incorporating Silicon-28 into SOI wafers made using either oxygen implantation or layer transfer technologies requires no change in the manufacturing processes developed for these wafers, the company said.
"While SOI wafers are known to reduce power requirements for devices, heat has been a large concern for certain applications and is expected to become an even larger, more critical consideration as chip manufacturers continue to push for more performance," said Stephen J. Burden, Isonics VP of semiconductor materials, in a statement. "Semiconductor manufacturers, eager to design the optimum thermal/electrical solution for their specific device, are becoming aware of the outstanding performance offered by the marriage of our high thermal conductivity silicon-28 and the film SOI wafer technology.
The wafers delivered to this customer were manufactured in cooperation with an existing thin-film SOI wafer supplier, Isonics said, instead of the company's thick-film SOI facility.

From "Semiconductor International 5-2002"

The *specific heat* c_p (of course for constant pressure) is not so important, but here are values anyway. In addition the **Debye temperature** Θ is shown, too

Material	Si	Ge	GaAs	SiO_2	Si_3N_4	Al
X_π **[J/g · K]** at room temperature	0,7	0,31	0,35			0,9
Θ **[K]**	645	374	362			

Other Properties

Here is a table found in the Net with some more non-electrical data

- Some of the numbers deviate from the numbers given above; e.g. the thermal expansion coefficient.
- That is just the way it is - if you look up anything, you will find different numbers. Often just a little bit different (melting points, for example), but sometimes quite different (as in the thermal expansion coefficient here).
- Reasons for this might be:
  1. The quantities compared are actually different. In the table above, the *linear* thermal expansion coefficient is given; in the table below it might be the expansion coefficient for the volume?
  2. Watch out for units. Conversion can be tricky, especially for some quaint old British imperial units still much beloved by the Americans, too.
  3. The samples might have been different. Giving the "conductivity" or "lifetime" for **Si** without some comments, obviously does not make much sense. How about other properties?
  4. The number is simply wrong.

Si Properties	
Refractive Index	3.4179 @ 10 µm ; 3,45
Reflective Loss	46.1 % @ 10 µm
Density	2,3291 g/cm^3
Melting Point	1420 °C
Molecular Weight	28.086
Thermal Conductivity	1,63 W/(cm K); 1,4 W/(cm K)
Specific Heat	0,703 J/(g K) @ 25 °C
Thermal Expansion	4.05×10^{-6} / K @ 10...50 °C
Hardness (Knoop)	1150 (Mohs 7)
Young's Modulus	131 GPa
Shear Modulus	79.9 GPa
Bulk Modulus	102 GPa
Rupture Modulus	340 MPa
Elastic Coefficient	C_{11} = 167 / C_{12} = 65 / C_{44} = 80 GPa
Dielectric Constant	13 @ f = 9.37 GHz