

A Preview of the 21st Century Failure and Yield Analysis Short Course

A totally new Failure and Yield Analysis Short Course and Handbook has been developed to maximize your productivity by:

**giving you the process for successfully analyzing these circuits
making it easier to understand the procedures and techniques
for performing analysis on complex circuits**

**providing you with the opportunity to learn from the experts who
created many of the techniques**

**The following pages provide an overview of the material typically
presented in this unique course. The course is complemented by
our 500+ page Handbook and a color CD ROM with a complete,
full-color copy of the Handbook and all of the slides presented in
the course.**

We invite comparison with any other course.

To find the schedule of classes and to register visit www.tsi-seminars.com

Learn the top-level process for both failure and yield analysis

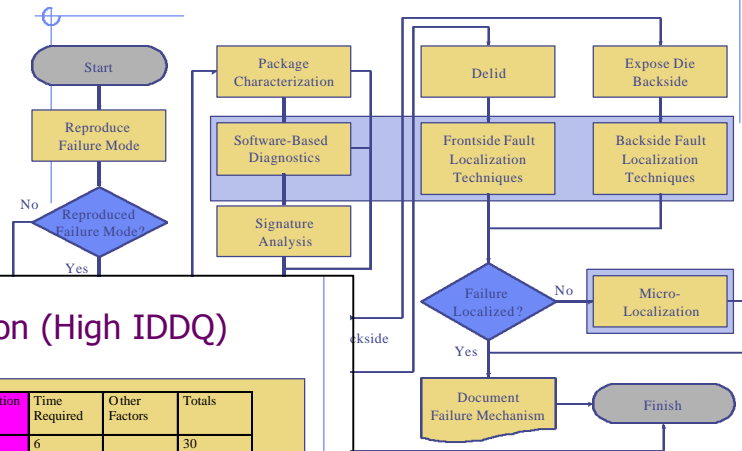
Philosophy of FA

- ◆ There are some basic philosophical principles for failure analysis
- ◆ Sherlock Holmes
 - The failure analyst is the detective searching for clues as to why the IC fails
 - Every clue is potentially important
 - Need to be organized
 - Story must make sense



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Packaged ICs - High Confidence



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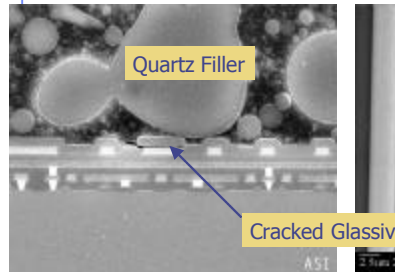
Example of Tool Selection (High IDDQ)

Technique	Availability	Potential Damage	Ease of Use	Information Gained	Time Required	Other Factors	Totals
Light Emission	Yes	9	7	8	6		30
Liquid Crystal	Yes	8	8	4	9		29
FMI	Yes	8	5	6	8		27
TIVA	Yes	9	3	7	7		26
CIVA	Yes	8	3	6	7		24
LIVA	Yes	9	3	4	7		23
E-Beam Probing	Yes	9	1	9	1		20
Laser Voltage Probe	No	5	1	9	1		16

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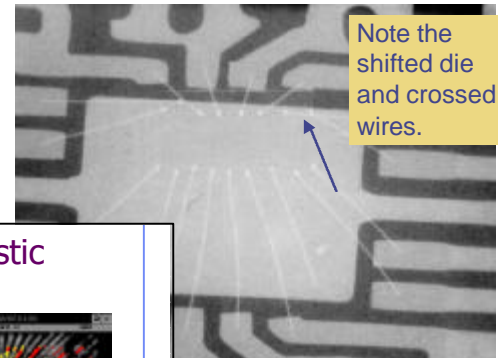
Learn packaging analysis techniques and failure mechanisms

Quartz Filler-Induced Failures - Photograph



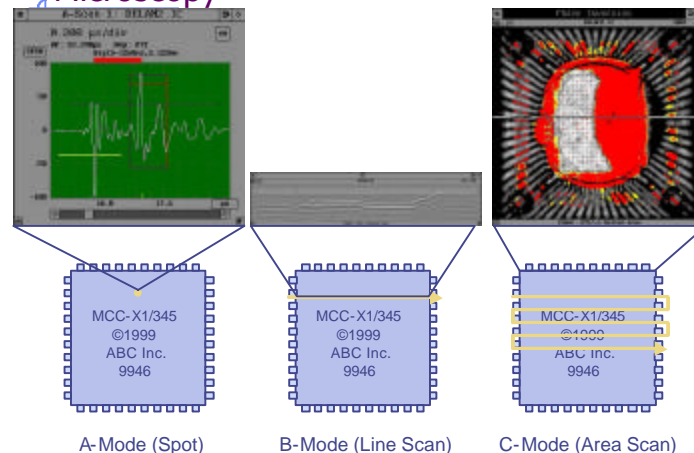
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X-radiography Photo



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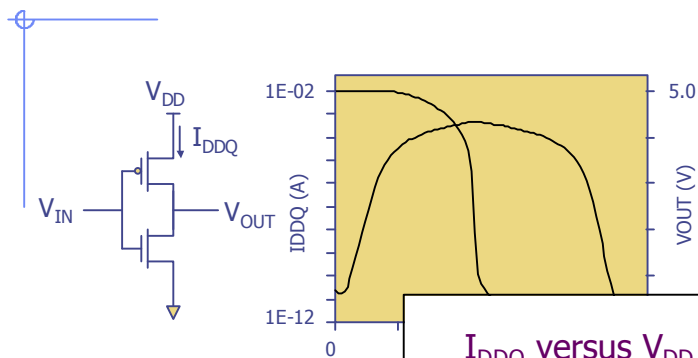
The Three Modes of Scanning Acoustic Microscopy



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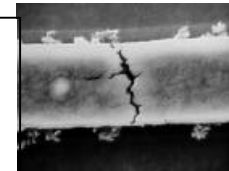
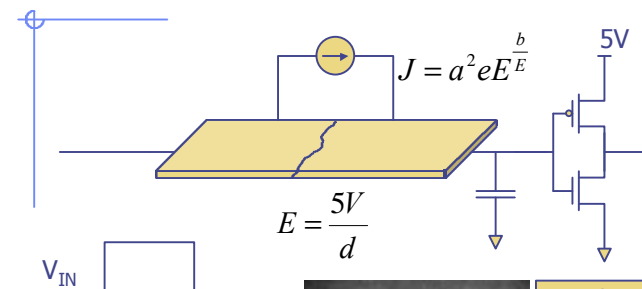
Learn the secrets of how to choose isolation techniques based on electrical signatures

CMOS Inverter



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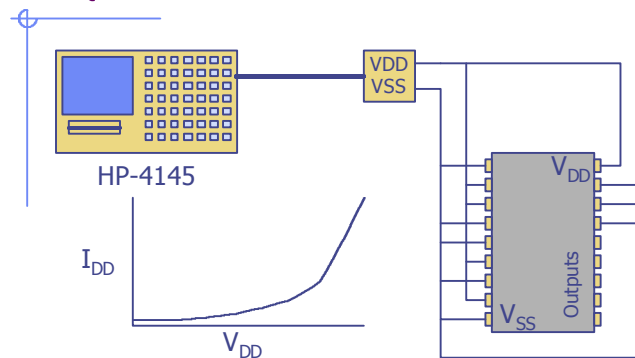
Small Tunneling Open Defect



- Metal stress voids
- Electromigration
- Unetched via oxide

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I_{DDQ} versus V_{DD} Failure Analysis



Place IC in non-contentive state, tie all inputs to VDD or VSS, Float all outputs, sweep from maximum supply voltage to zero

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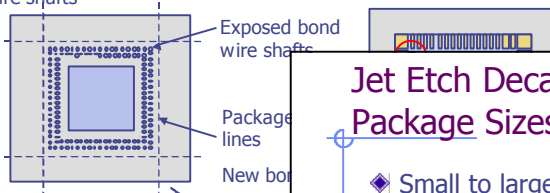
Learn how to decapsulate packages and prepare samples from the backside

Access to Chip-Scale Packages

Step 1: Grind/polish through bumps and circuit board and first die (if appropriate)

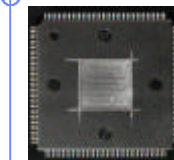
Step 2: Cut excess material away from BGA package

Step 3: Place remaining BGA package in PGA package and rebond to the appropriate exposed wire shafts

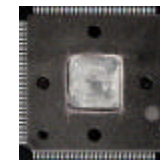


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CNC milling: Process steps



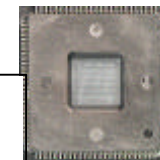
Chip size marked, plastic milled



Plastic removed down to the leadframe



Leadframe removed down to the glue



Milling of the Si substrate



Si substrate polished

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Jet Etch Decapsulation Different Package Sizes

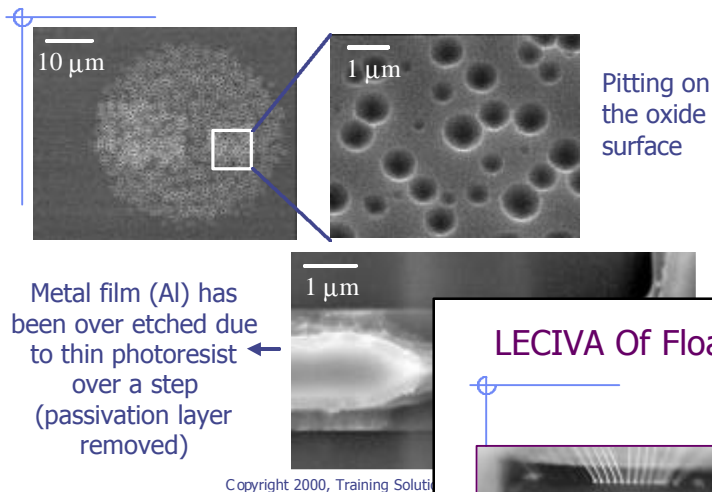
Small to large package and die decapsulation



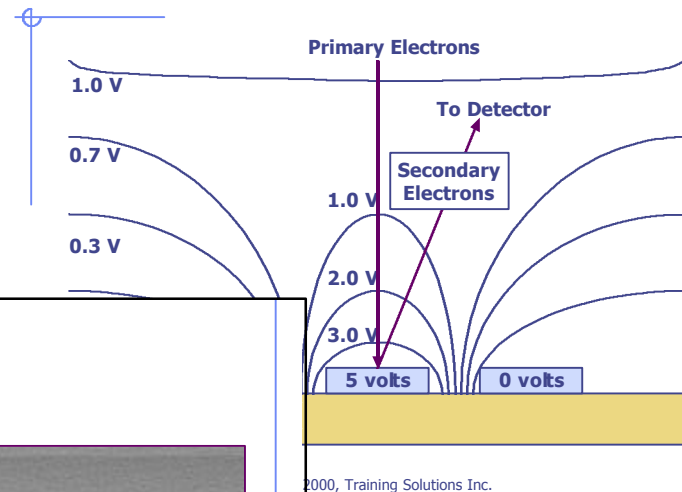
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Learn how to use an SEM and the many techniques that can be performed with it

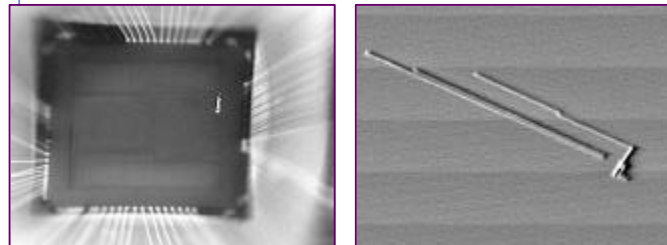
Surface Imaging using SEM



Principle Behind Biased Voltage Contrast



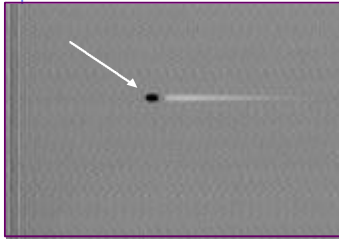
LECIVA Of Floating NAND



- ♦ 3 input NAND, floating inputs
- ♦ shows M3 and M2, 0.5 micron technology

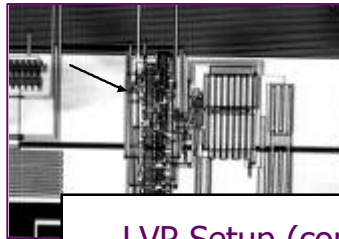
Learn about optical techniques and their power to facilitate backside analysis

IR LIVA Backside Example: Open Metal to Silicon Contact

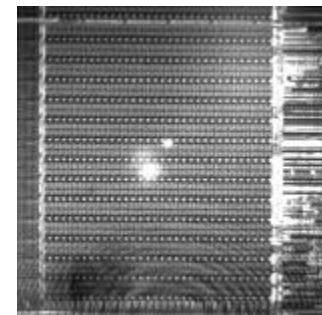
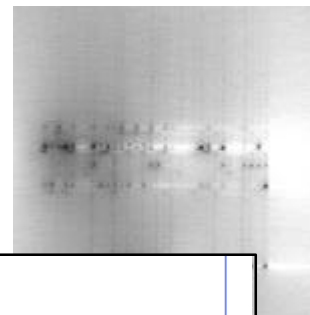


Backside IR LIVA image of defect

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Microprocessor Failure (Backside): Suspected Capacitor Damage

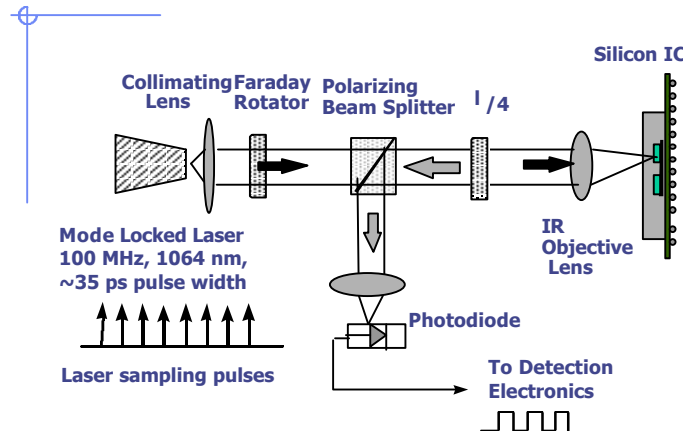


Reflected image

Technology)

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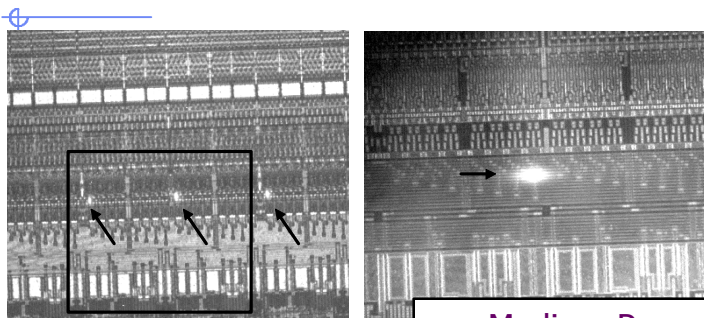
LVP Setup (cont.)



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Learn about thermal techniques more sensitive than you re currently using

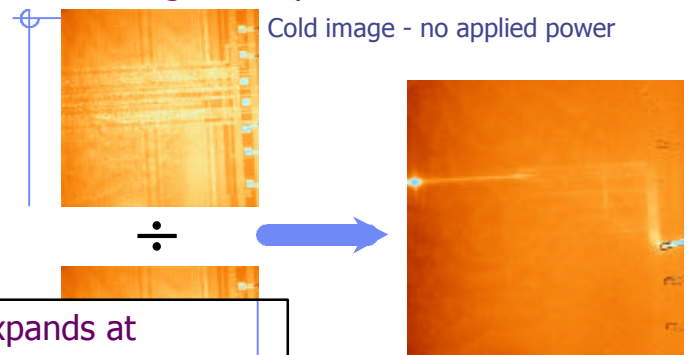
Example 3



Overlay of light-emission and reflected light images showing light-emitting regions.

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FMI Image Example

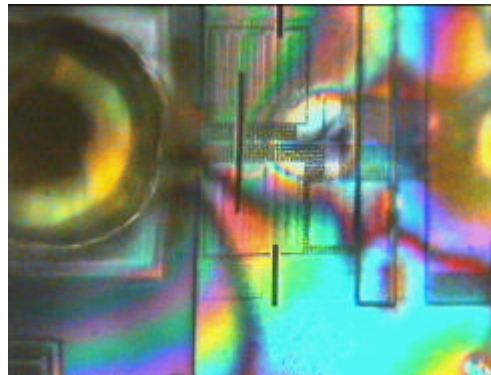


FMI image

Hot image - with applied power

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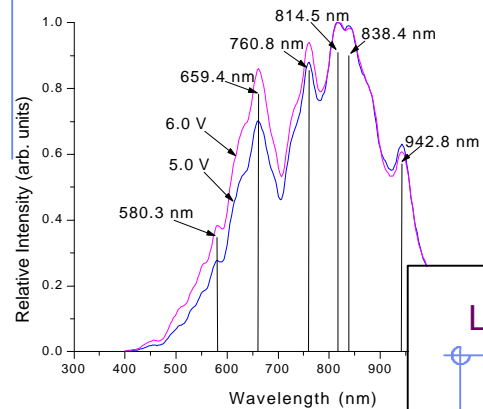
Medium Power - Bubble expands at Failure Site



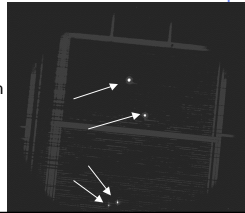
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Unlock the power of photon emission microscopy

Gate Oxide Failure Example

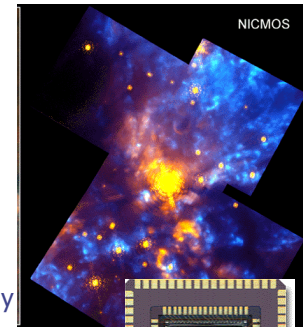


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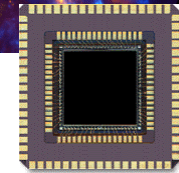


NICMOS Array

- ◆ NICMOS - Near Infrared Camera Multi-Object Spectrograph
- ◆ Now called PICNIC and has improved noise performance
- ◆ Optimized for use between 800 & 2500 nm
- ◆ 256 by 256 pixel HgCdTe array
- ◆ First Array with Si-CCD level



on Hubble
February 1997

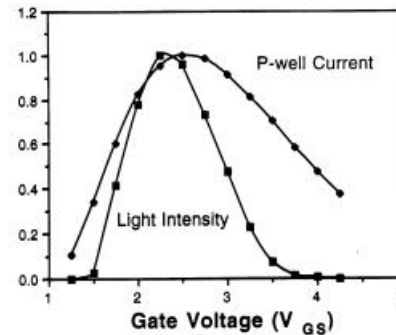


<http://www.rsc.rockwell.com/>

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Light Emission Correlates to I_{SUB}

- ◆ Light emission peak near P-well current peak
- ◆ Transistor must be in saturation to emit detectable light



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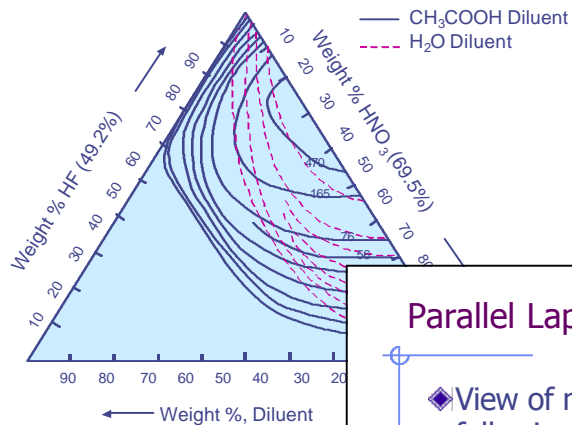
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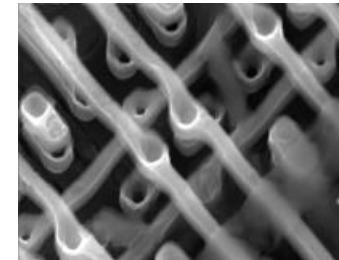
Learn how to deprocess an integrated circuit effectively

Isoetch Curves for Silicon (HF:HNO₃:diluent system)



Passivation Removal

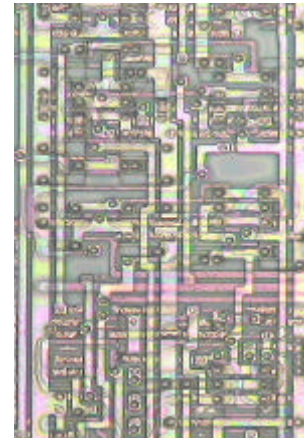
- ◆ Provides for the unobstructed inspection or microprobing of underlying metallization and to highlight other details of the circuitry without metallization attack.



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Parallel Lapping (cont.)

- ◆ View of metal 1 following parallel lapping to remove top metal.



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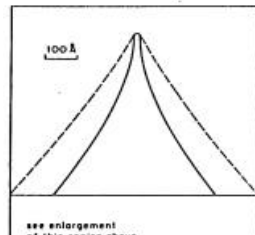
Understand the many uses of the Focused Ion Beam system

Liquid Metal Ion Source

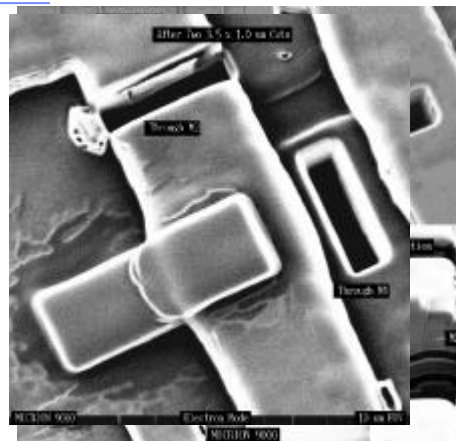


From FEI Product Literature

D. R.
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Circuit Edits



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TEM Sample Preparation : Lift Out Technique

- ♦ Create TEM lamella in FIB
- ♦ Undercut and remove with microprobe
- ♦ No need for grinding

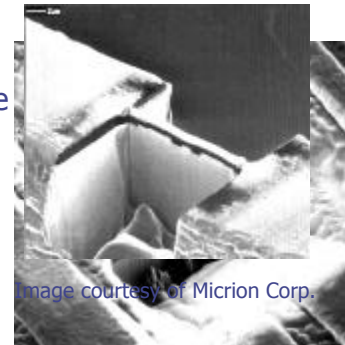
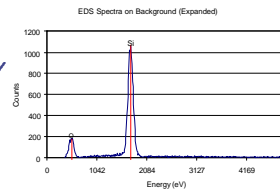
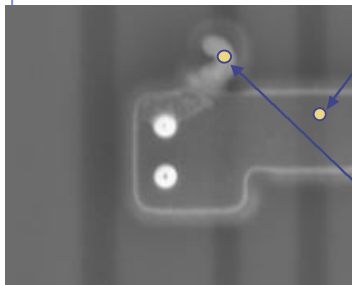


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Learn about the TEM, SIMS, EDS, AES, AFM and more

An Example Application (Foreign Material)



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TEM Imaging

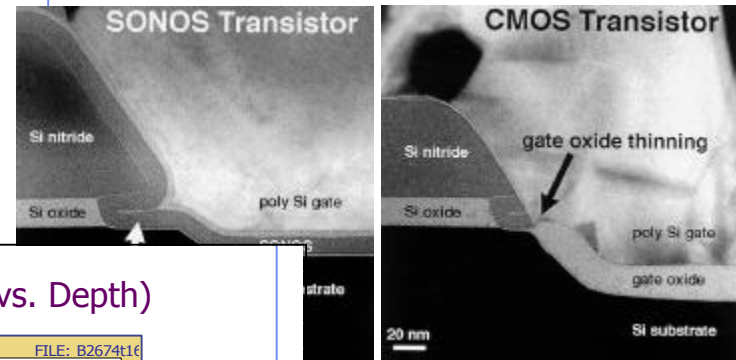
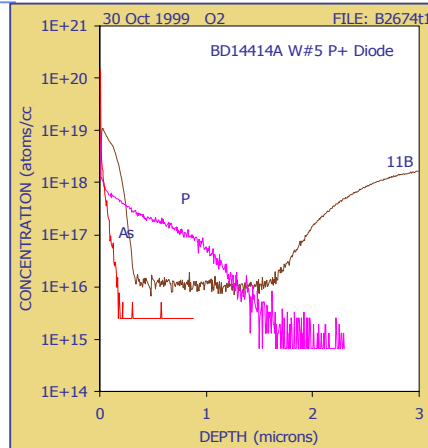


Image by Tom Headley, Dept. 1822

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SIMS Data (Concentration vs. Depth)



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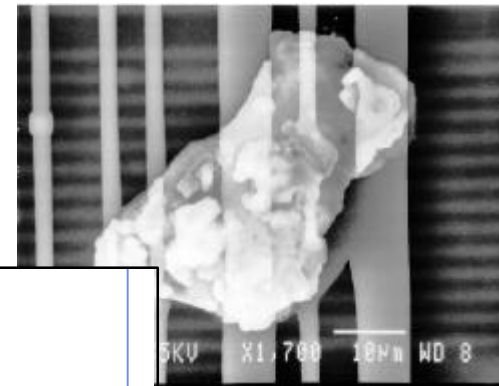
In addition, we cover Case Histories, Failure Mechanisms, and more!

Case History 3 - Failure Analysis of ASIC Burn-In Failures

Christopher Henderson
Michael Strizich

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Particle Defects



Worst Case Particle at Metal-3 Patterning

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Websites for Failure Analysis

- ◆ EDFAS <http://www.edfas.org>
- ◆ Charles Evans <http://www.cea.com>
- ◆ IBM Analytical Services
<http://www.chips.ibm.com/services/asg/index.html>
- ◆ March Instruments <http://www.plasmod.com/>
- ◆ Semiconductor International
<http://www.semiconductor.net/semiconductor/lores/index.html>
- ◆ Argonne National Laboratory Microscopy Site
<http://www.amc.anl.gov/>
- ◆ Digital Instruments <http://www.di.com/>
- ◆ SIMS Web Server
<http://www.simsworkshop.org/default.ncl>

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